

11/03 Add DC-IN Cable P/N : DC301009N00 12/04 Change PJP1 to JDCIN1
11/18 Change PCB P/N from DA60000G300 to DA60000G200
02/26 Change LA-6101P P/N from DA60000G200 to DA60000G210
02/26 Add DAZ P/N and other small board P/N
02/26 Change DAZ P/N from DAZ0D9001001 to DAZ0D900101

Compal Confidential

NAU00 LA-6101P Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

SV M/B

2010-03-09

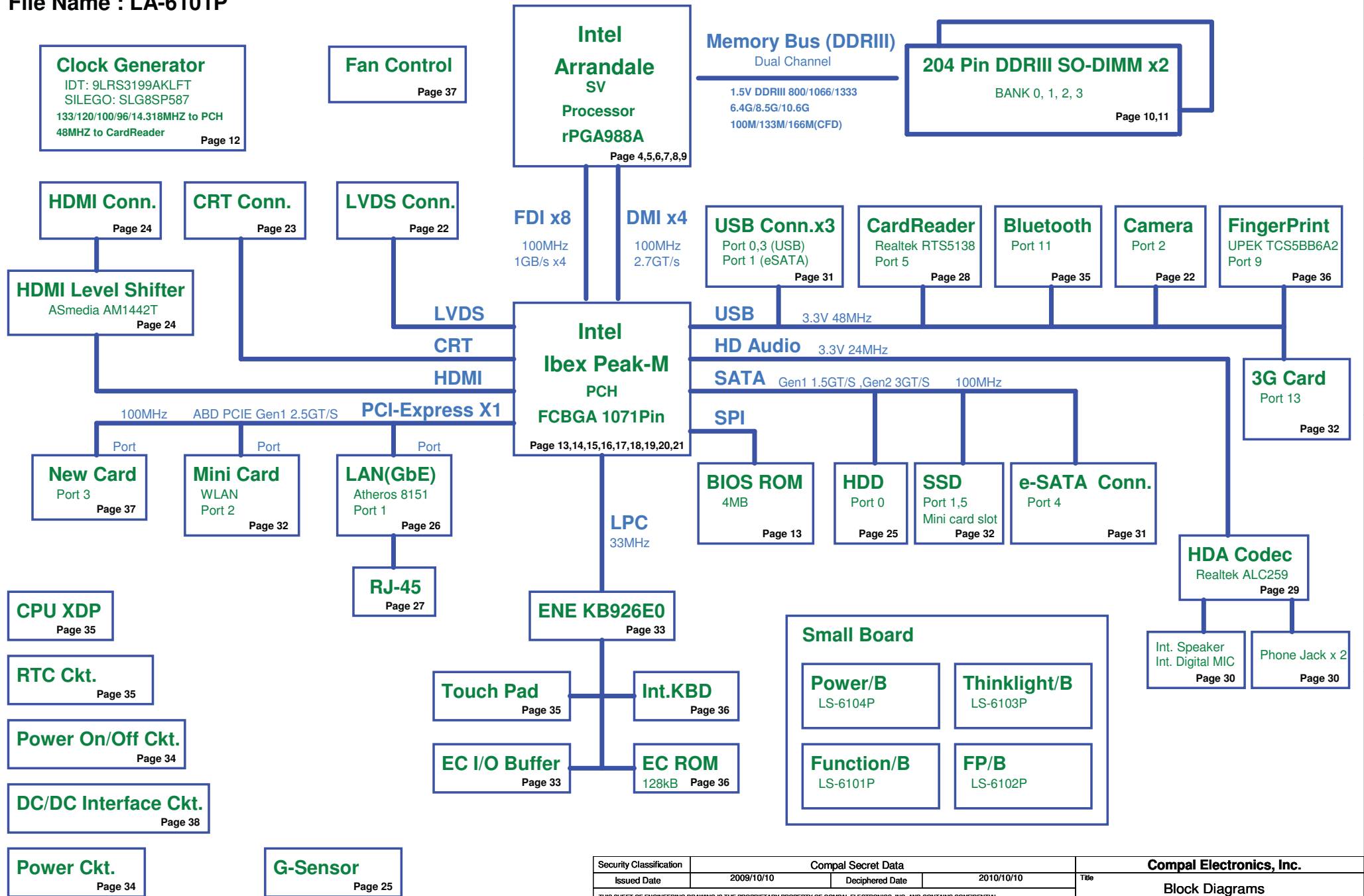
Rev : 1.0

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Model Name : NAU00

File Name : LA-6101P



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Size B	Document Number	NAU00 M/B LA-6101P Schematics		Rev 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727	0101 1100b
ISL90728	0111 1100b

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

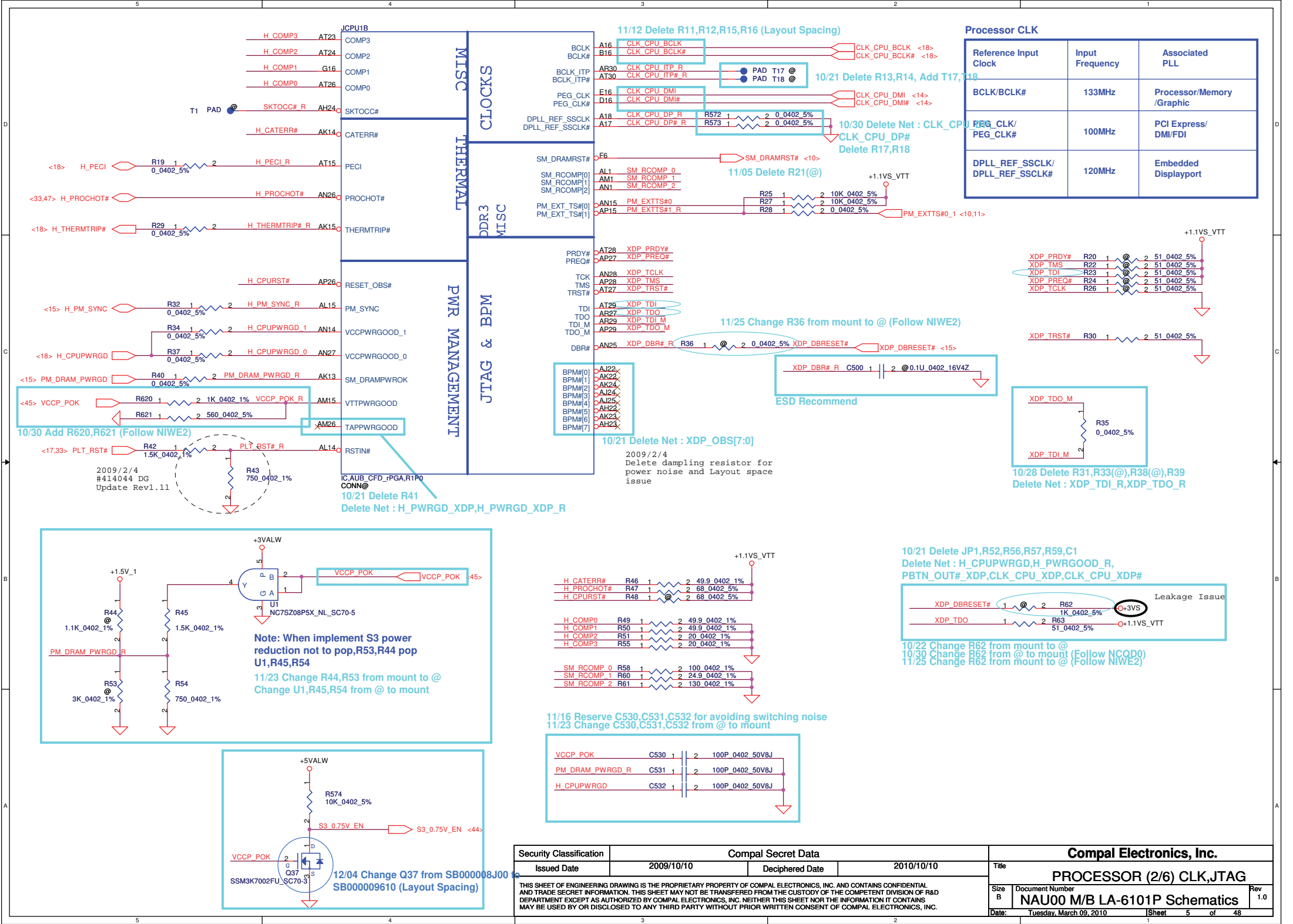
Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

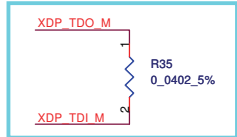
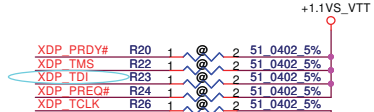
BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

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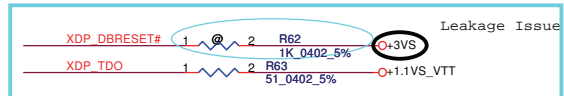


Processor CLK		
Reference Input Clock	Input Frequency	Associated PLL
BCLK/BCLK#	133MHz	Processor/Memory /Graphic
PEG_CLK/ PEG_CLK#	100MHz	PCI Express/ DMI/FDI
DPLL_REF_SSCLK/ DPLL_REF_SSCLK#	120MHz	Embedded Displayport

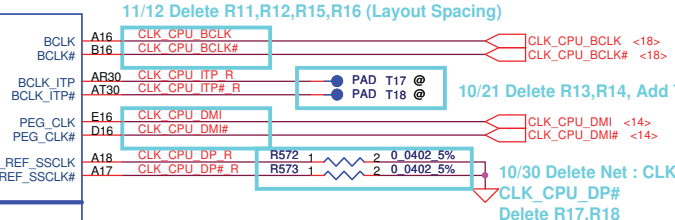


10/28 Delete R31,R33(@),R35(@),R39
Delete Net : XDP_TDI_R,XDP_TDO_R

10/21 Delete JP1,R52,R56,R57,R59,C1
Delete Net : H_CPUPWRGD,H_PWRGOOD_R,
PBTN_OUT#_XDP,CLK_CPU_XDP,CLK_CPU_XDP#



10/22 Change R62 from mount to @
10/30 Change R62 from @ to mount (Follow NIWE2)
11/25 Change R62 from mount to @ (Follow NIWE2)



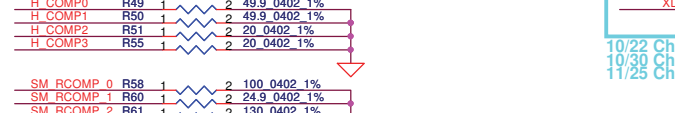
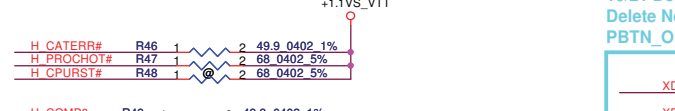
11/12 Delete R11,R12,R15,R16 (Layout Spacing)
10/21 Delete R13,R14, Add T17,T18
10/30 Delete Net : CLK_CPU_PEG_CLK/
Delete R17,R18
11/05 Delete R21(@)



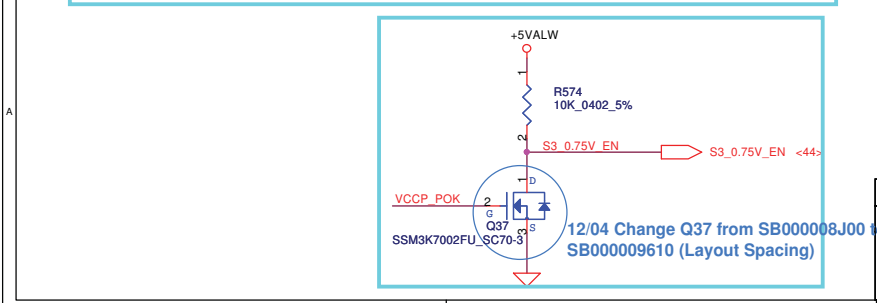
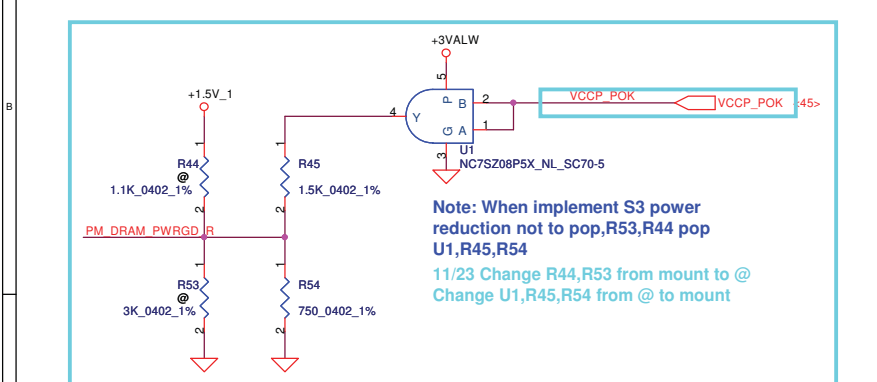
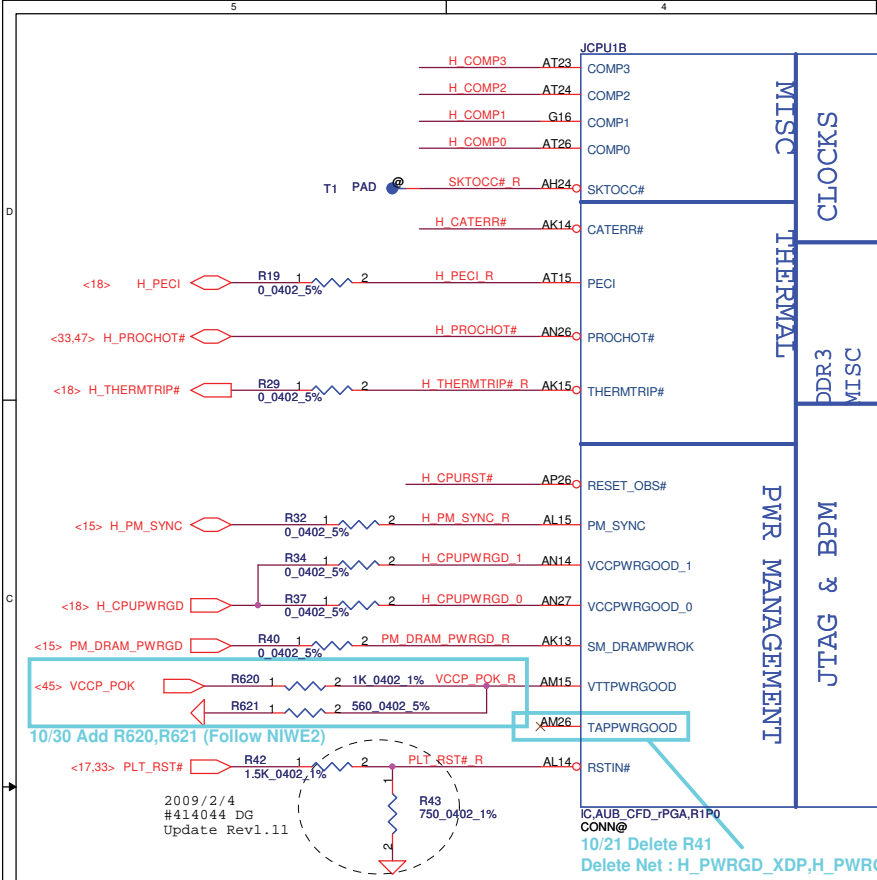
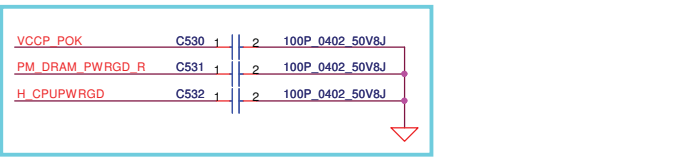
11/25 Change R36 from mount to @ (Follow NIWE2)
ESD Recommend



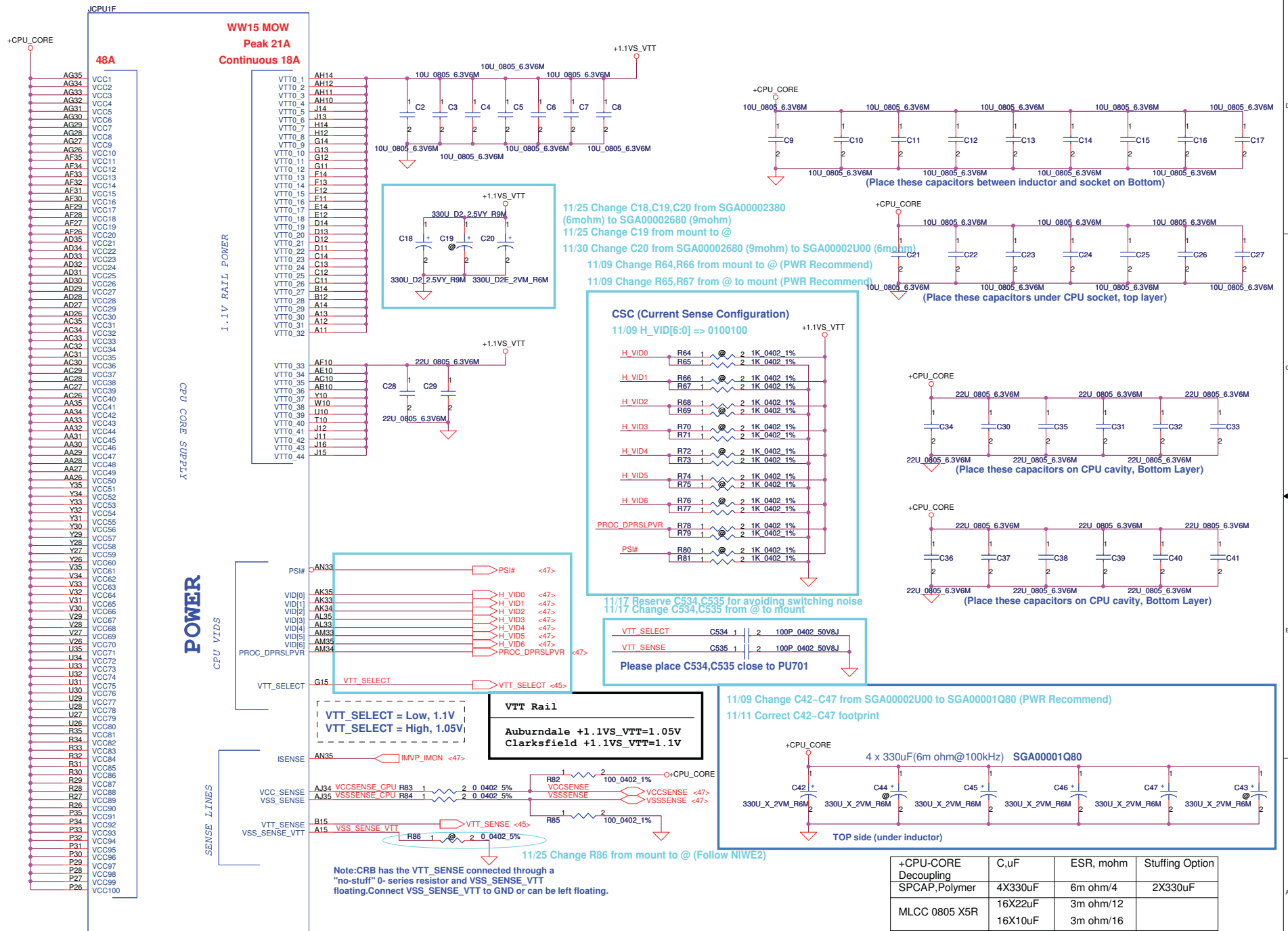
10/21 Delete Net : XDP_OBS[7:0]
2009/2/4
Delete damping resistor for
power noise and Layout space
issue

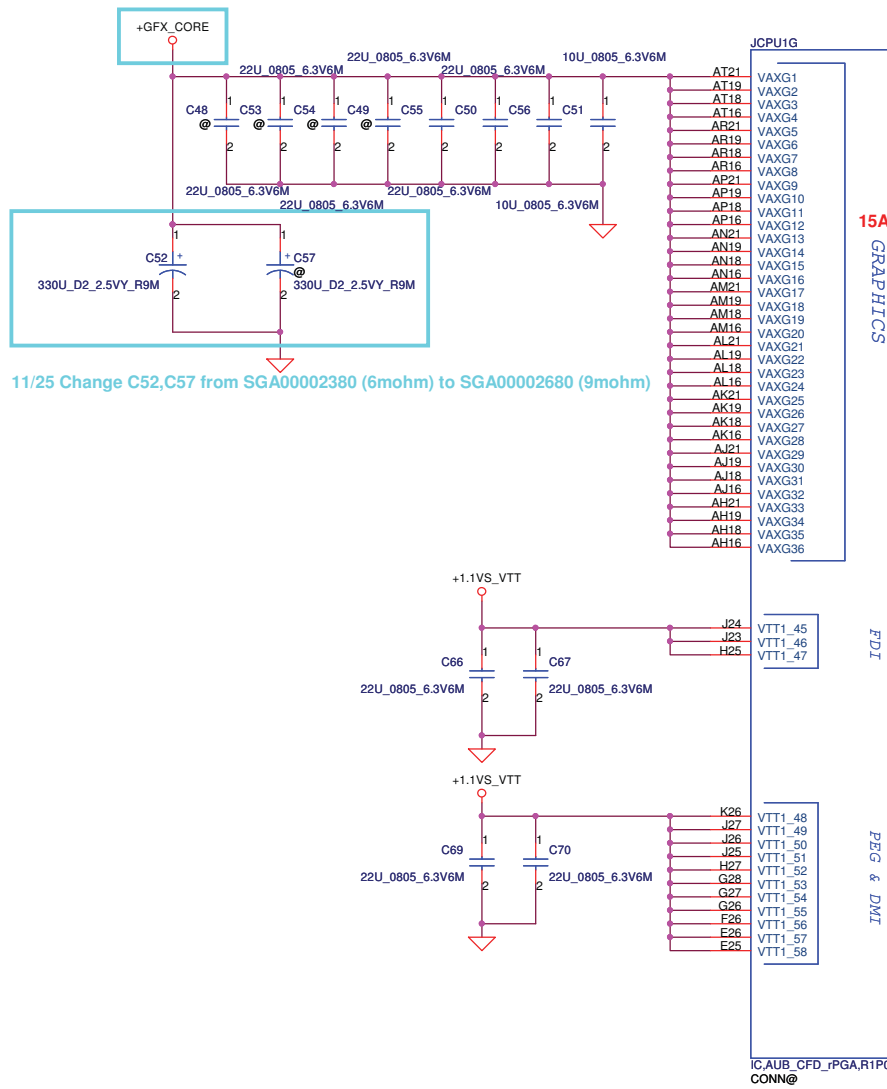


11/16 Reserve C530,C531,C532 for avoiding switching noise
11/23 Change C530,C531,C532 from @ to mount



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POWER

3A
1.5V RAILS
1.1V
0.6A

15A
GRAPHICS

SENSE LINES
GRAPHICS VIDS

DDR3 - 1.5V RAILS

1.1V

0.6A

1.8V

1.5V

1.1V

0.6A

1.8V

1.5V

1.1V

0.6A

1.8V

1.5V

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1.5V

1.1V

0.6A

1.8V

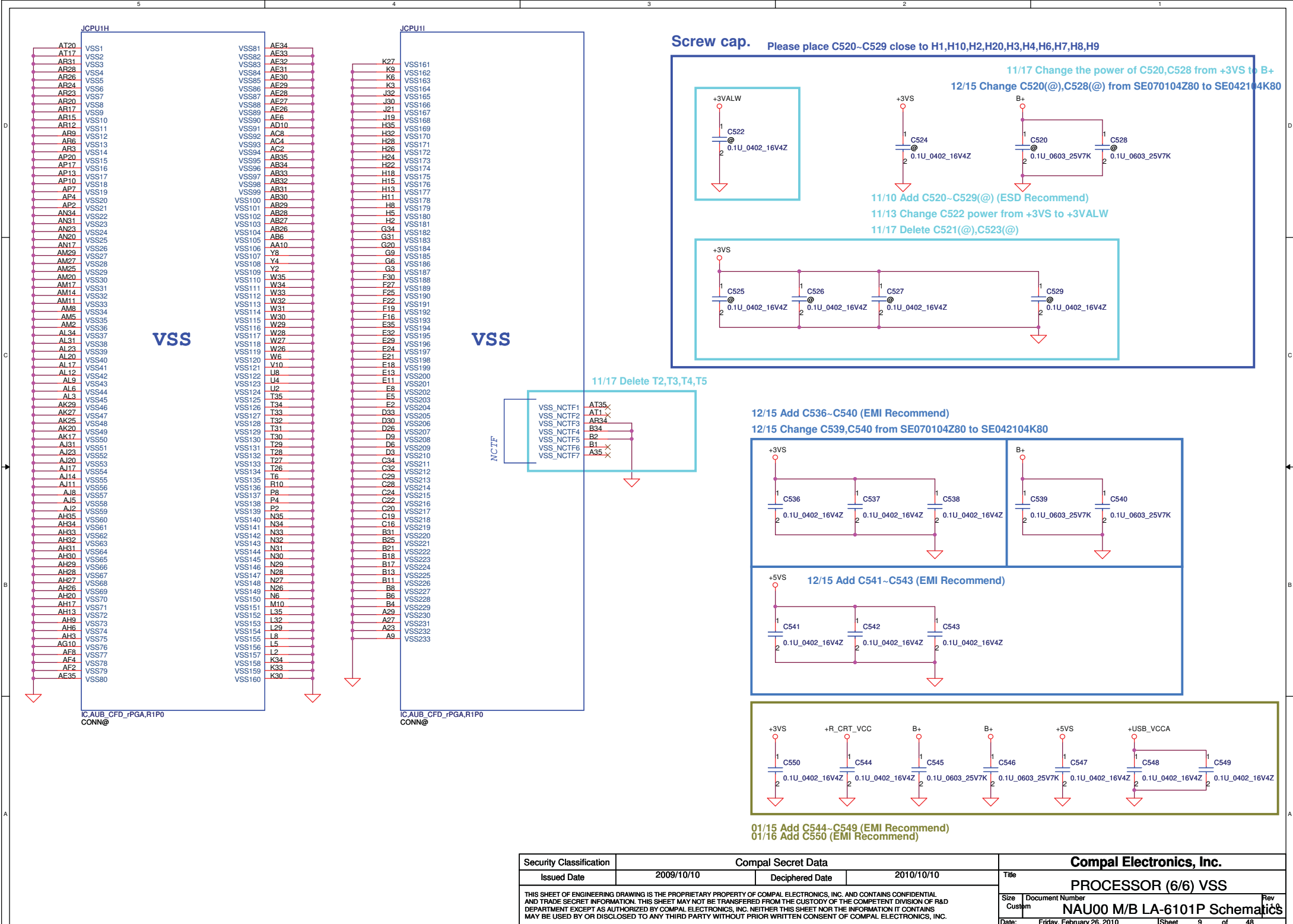
1.5V

1.1V

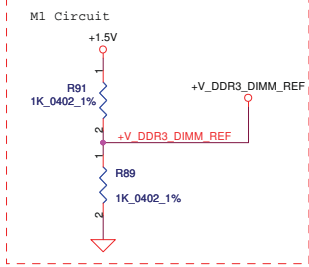
0.6A

1.8V

1.5V



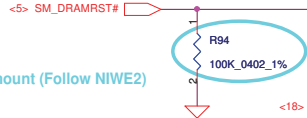
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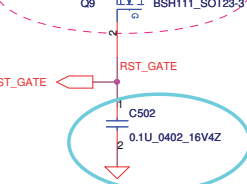
2009/04/13
For Arrandale ,it should be use M1 Circuit
For Clarksfield ,it should be use M3 Circuit
DG V1.52

- <6> DDR_A_DQS#[0..7]
- <6> DDR_A_D[0..63]
- <6> DDR_A_DM[0..7]
- <6> DDR_A_DQS[0..7]
- <6> DDR_A_MA[0..15]

11/05 Change R94 from @ to mount (Follow NIWE2)



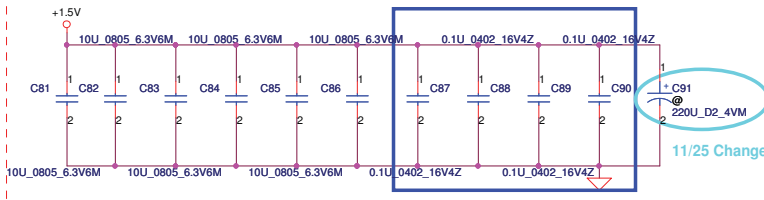
11/10 Change C78 from SE103225Z80 to SE049225Z80
10/21 Change R93 from @ to mount



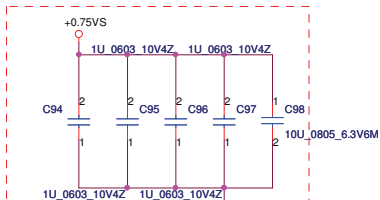
10/22 Add C502 at RST_GATE
(Intel 425302_CalPELLa_S3PowerReduction_WhitePaper_Rev1.0)
11/09 Change C502 from 0.047uF to 0.1uF
11/23 Change R92 from mount to @
Change Q9 from @ to mount

Layout Note:
Place near JDIMM1

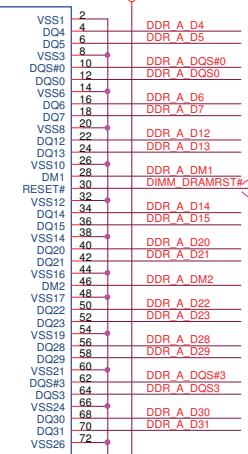
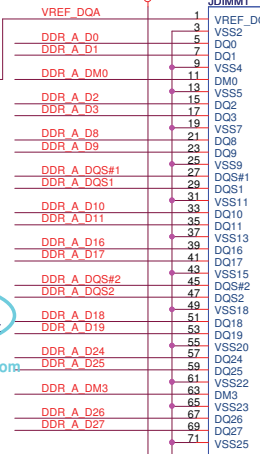
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



- <6> DDR_A_CKE0
- <6> DDR_A_BS2
- <6> DDR_A_CLK0
- <6> DDR_A_CLK#
- <6> DDR_A_MA10
- <6> DDR_A_BS0
- <6> DDR_A_WE#
- <6> DDR_A_CAS#
- <6> DDR_A_MA13
- <6> DDR_A_CS1#



- DDR A D4
- DDR A D5
- DDR A DQS#0
- DDR A DQS0
- DDR A D6
- DDR A D7
- DDR A D12
- DDR A D13
- DDR A DM1
- DIMM_DRAMRST#
- DDR A D14
- DDR A D15
- DDR A D20
- DDR A D21
- DDR A DM2
- DDR A D22
- DDR A D23
- DDR A D28
- DDR A D29
- DDR A DQS#3
- DDR A DQS3
- DDR A D30
- DDR A D31
- DDR A CKE1
- DDR A CKE1 <6>
- DDR A MA15
- DDR A MA14
- DDR A MA11
- DDR A MA7
- DDR A MA6
- DDR A MA4
- DDR A MA2
- DDR A MA0
- DDR A CLK1
- DDR A CLK1#
- DDR A BS1
- DDR A BS1#
- DDR A CS0#
- DDR A CS0#
- DDR A ODT0
- DDR A ODT1
- DDR A ODT1#
- DDR A D36
- DDR A D37
- DDR A DM4
- DDR A D38
- DDR A D39
- DDR A D44
- DDR A D45
- DDR A DQS#5
- DDR A DQS5
- DDR A D46
- DDR A D47
- DDR A D52
- DDR A D53
- DDR A DM6
- DDR A D54
- DDR A D55
- DDR A D60
- DDR A D61
- DDR A DQS#7
- DDR A DQS7
- DDR A D62
- DDR A D63
- PM_EXTT#0
- PM_EXTT#0 <1,11>
- D_CK_SDATA
- D_CK_SDATA <11,12>
- D_CK_SCLK
- D_CK_SCLK <11,12>

DDR3 SO-DIMM A
Standard Type
H = 4.0mm

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<6> DDR_B_DQS#[0..7]

<6> DDR_B_D[0..63]

<6> DDR_B_DM[0..7]

<6> DDR_B_DQS[0..7]

<6> DDR_B_MA[0..15]

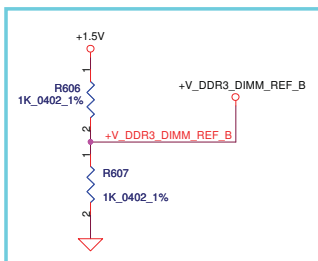
2009/04/13
For Arrandale, it should be use M1 Circuit
For Clarkfield, it should be use M3 Circuit
DG V1.52

+V_DDR3_DIMM_REF_B

M1 Circuit

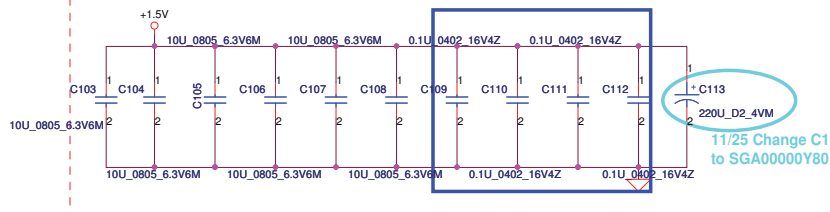
C99

11/10 Change C99 from
SE103225Z80 to
SE049225Z80



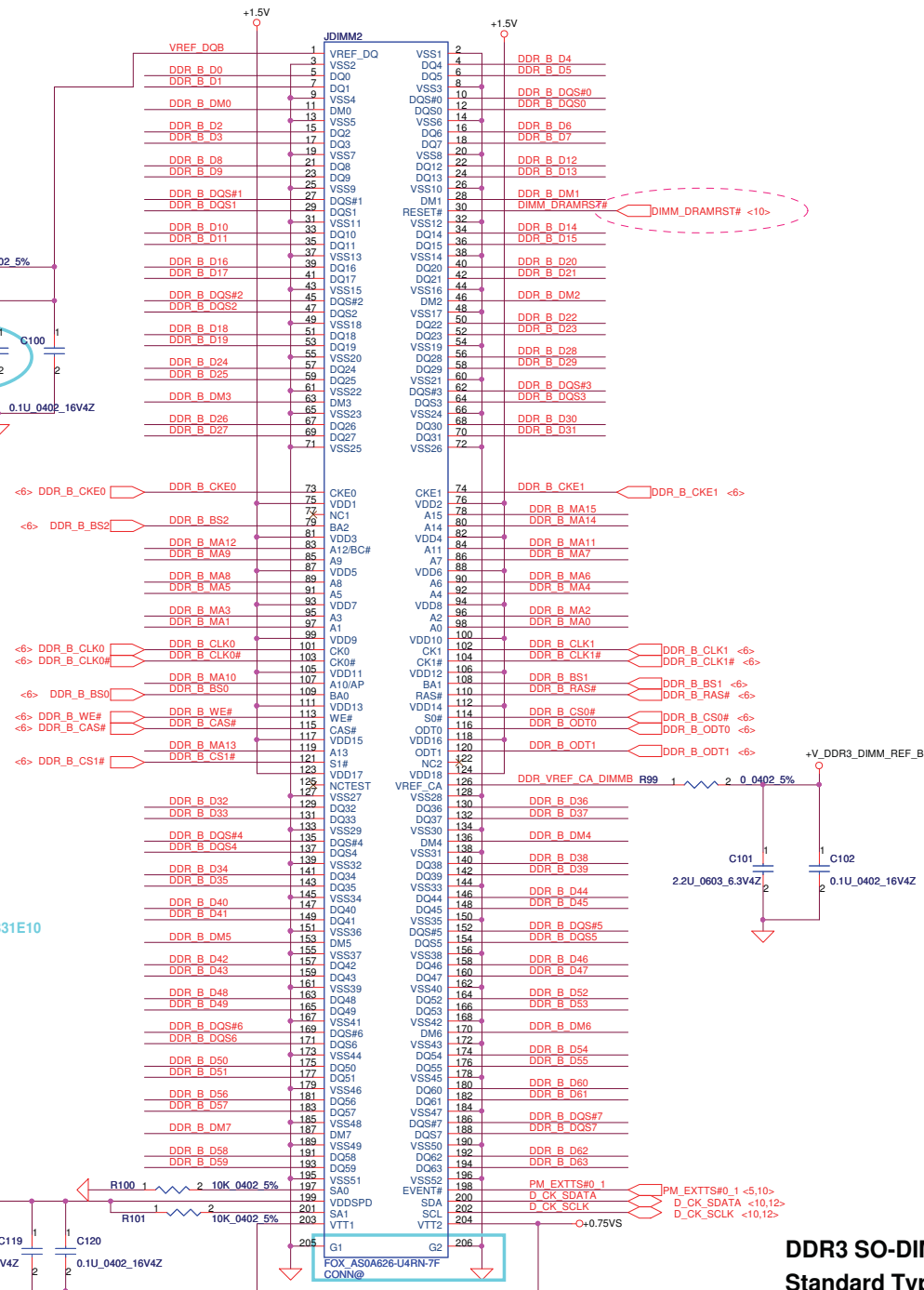
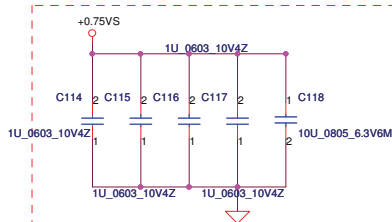
Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



11/25 Change C113 from
SGA20331E10
to SGA0000Y80

Layout Note:
Place near JDIMM2.203 & JDIMM2.204

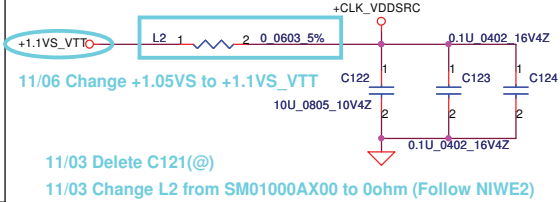


DDR3 SO-DIMM B
Standard Type

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2009/10/10	Deciphered Date	2010/08/25	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>				Title	
				DDR3III-SODIMM SLOT2	
				Size	Document Number
				NAU00 M/B LA-6101P Schematics	Rev 1.0
				Date:	Tuesday, March 09, 2010

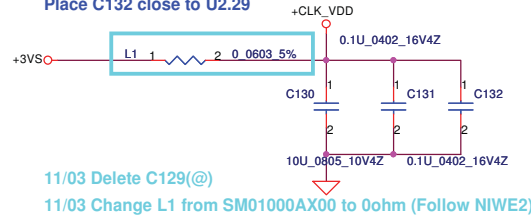
Layout note:

Place C122 close to L2
Place C123 close to U2.15
Place C124 close to U2.18



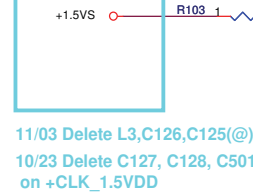
Layout note:

Place C130 close to L1
Place C131 close to U2.5
Place C132 close to U2.29



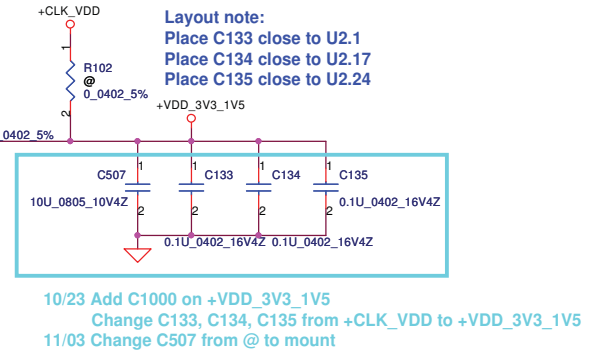
Layout note:

Place C507 close to R103



Layout note:

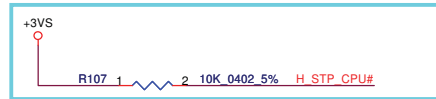
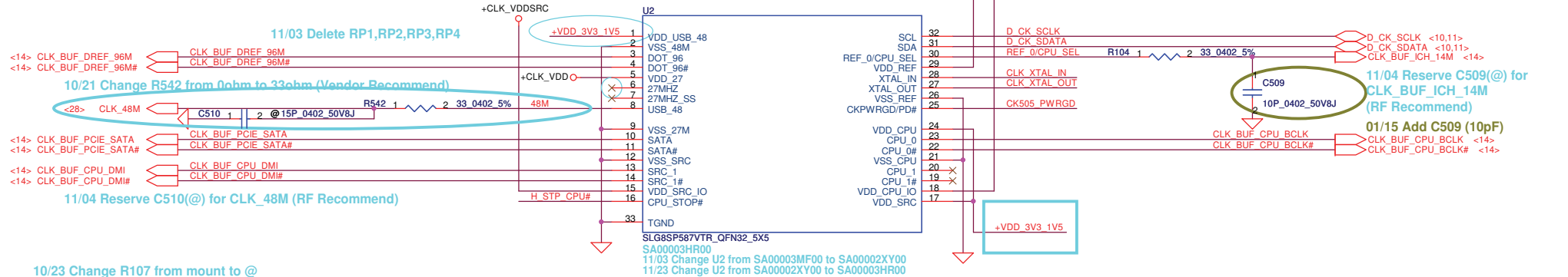
Place C133 close to U2.1
Place C134 close to U2.17
Place C135 close to U2.24



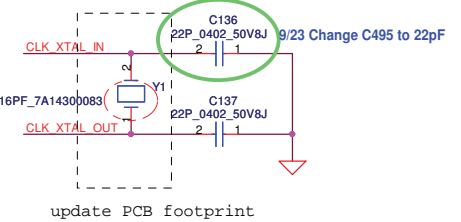
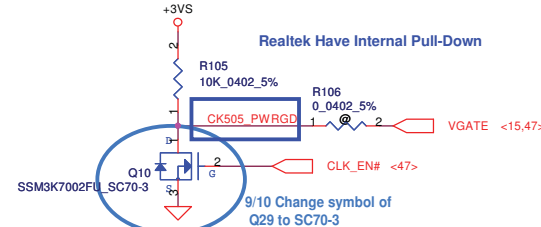
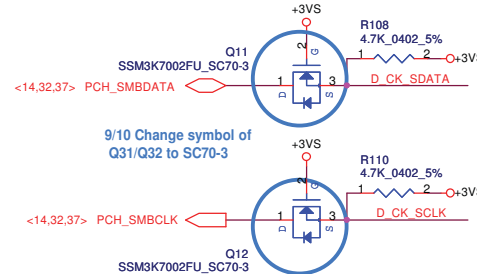
Type	R102	R103
Standard	Mount	@
Low Power	@	Mount

10/23 Change U2 Pin1,17,24
Net Name to +VDD_3V3_1V5

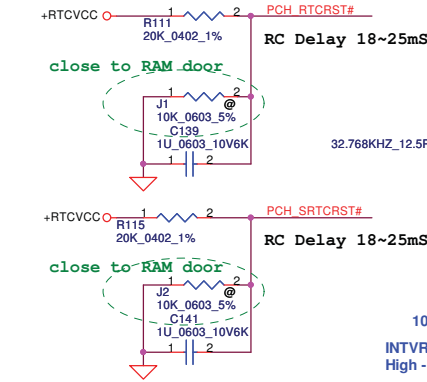
Clock Generator



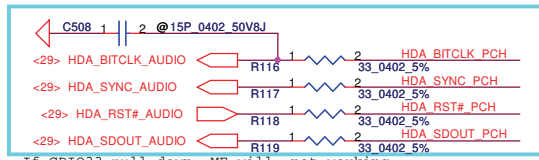
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



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Issued Date		2009/10/10	Deciphered Date	2010/10/10		Title	
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					Size	Document Number	Rev
					Custom	NAU00 M/B LA-6101P Schematics	1.0
Date:		Tuesday, March 09, 2010		Sheet	12	of 48	



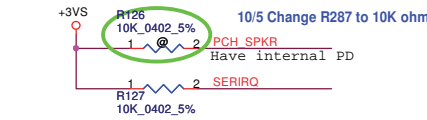
HDA for AUDIO 11/04 Reserve C508(@) for BITCLK (RF Recommend)



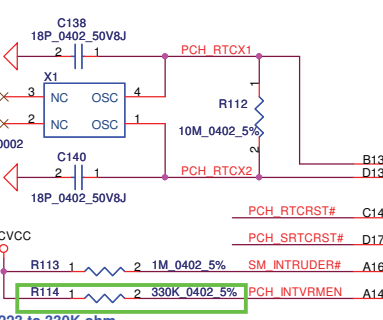
If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull under door.

11/10 Delete Q13,R120,R121 (Follow NIWE2)

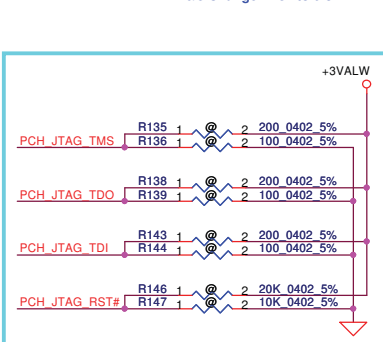
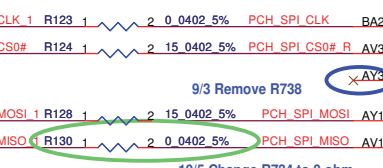
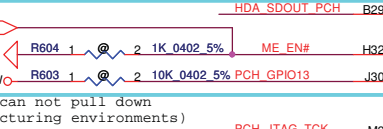
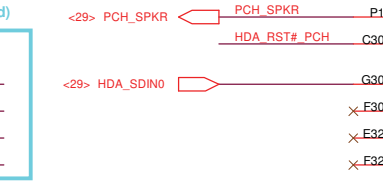
GPIO33 can not pull down (manufacturing environments)



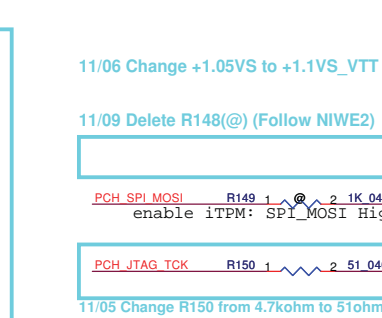
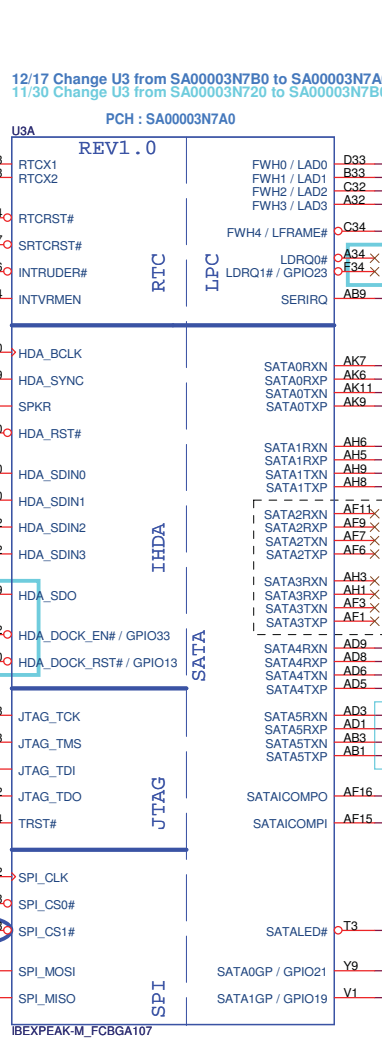
PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	★ MP
PCH_JTAG_TDO	R138	No Install	200ohm	No Install
	R139	No Install	100ohm	No Install
PCH_JTAG_TMS	R135	200ohm	200ohm	No Install
	R136	100ohm	100ohm	No Install
PCH_JTAG_TDI	R143	200ohm	200ohm	No Install
	R144	100ohm	100ohm	No Install
PCH_JTAG_TCK	R150	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R146	20Kohm	20Kohm	No Install
	R147	10Kohm	10Kohm	No Install



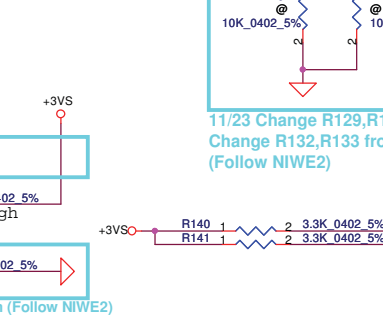
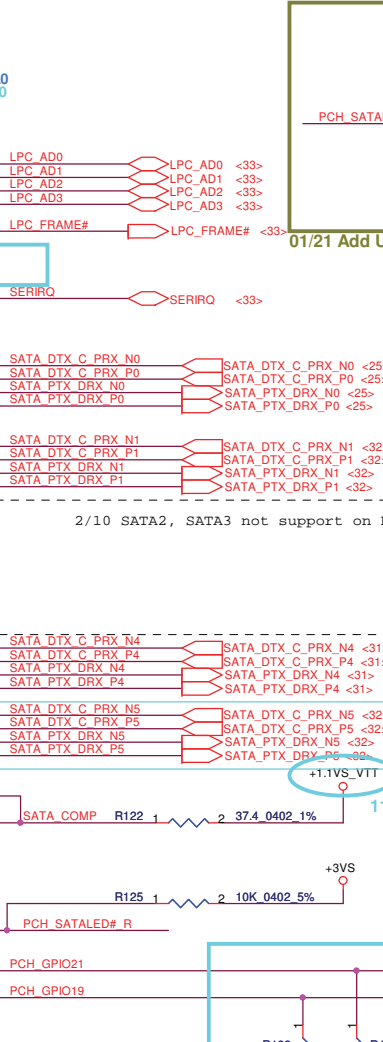
10/5 Change R223 to 330K ohm
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs



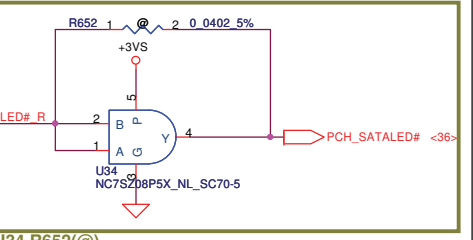
11/05 Change R135,R136,R138,R139,R143,R144,R146,R147 from mount to @ (Follow NIWE2)
11/10 Delete R134(@),R137(@),R142(@),R145(@)



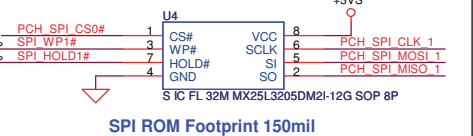
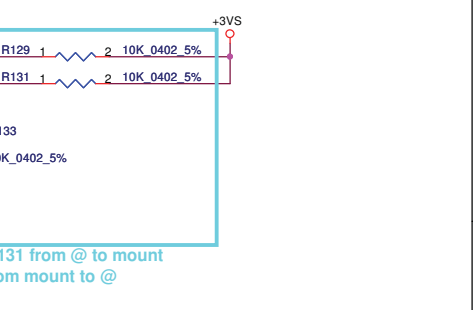
11/05 Change R150 from 4.7kohm to 51ohm (Follow NIWE2)



11/05 Change R150 from 4.7kohm to 51ohm (Follow NIWE2)



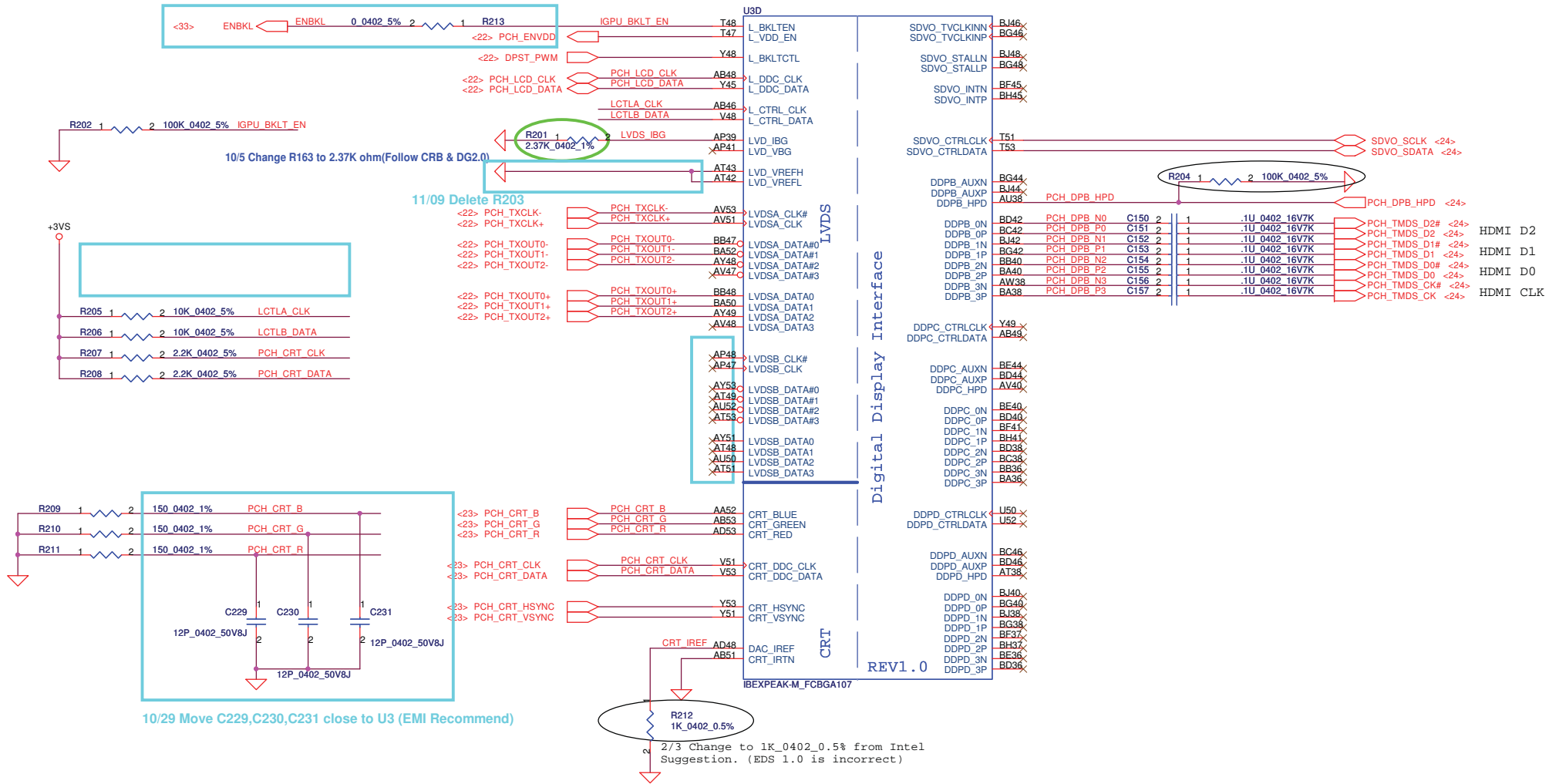
01/21 Add U34,R652(@)

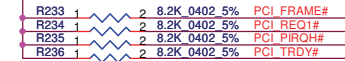
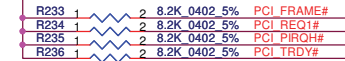
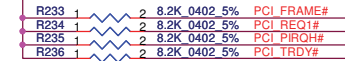
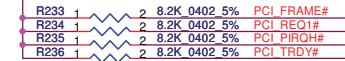
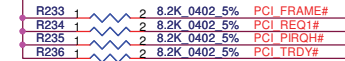
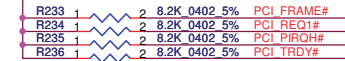
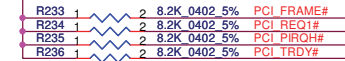
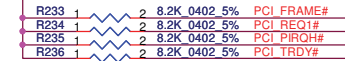
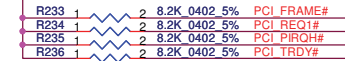
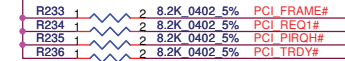
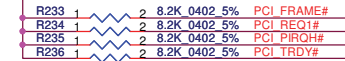
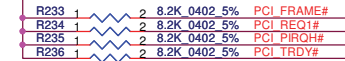
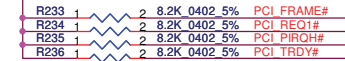
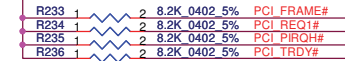
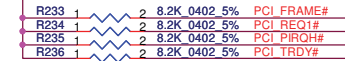
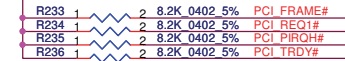
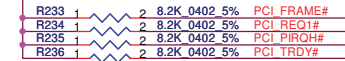
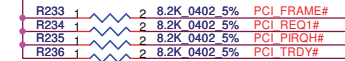
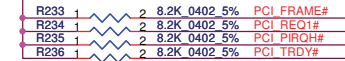
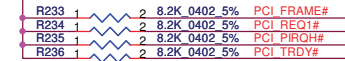
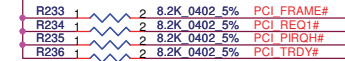
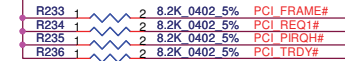
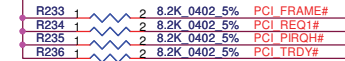
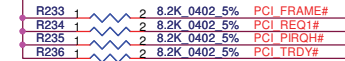
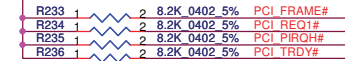
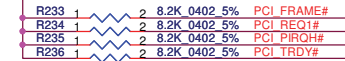
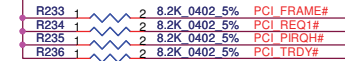
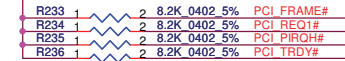
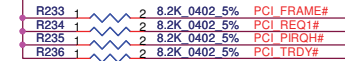
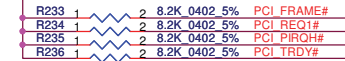
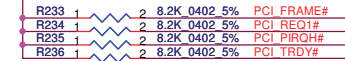
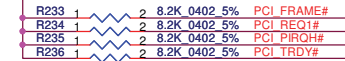
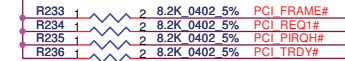
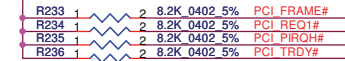
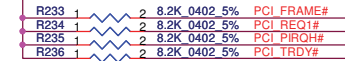
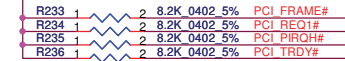
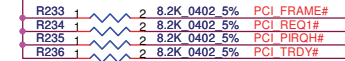
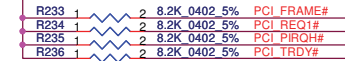
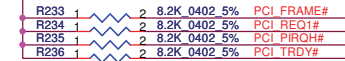
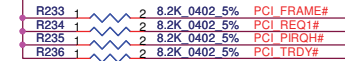
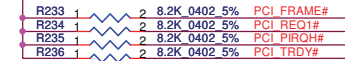
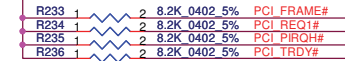
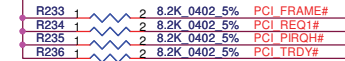
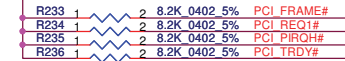
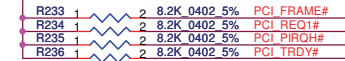
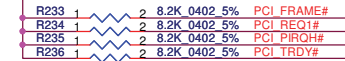
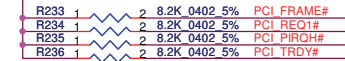
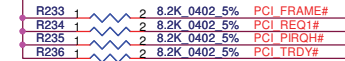
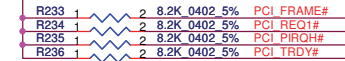
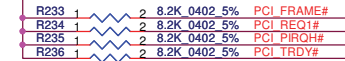
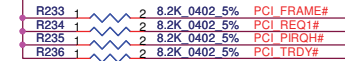
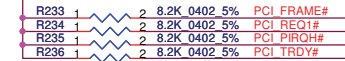
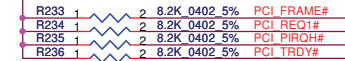
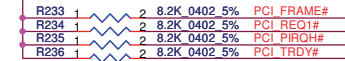
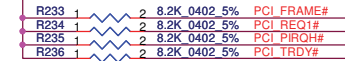
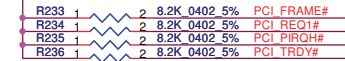
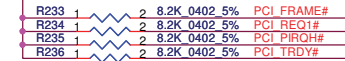
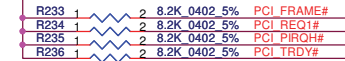
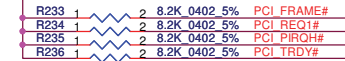
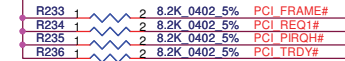
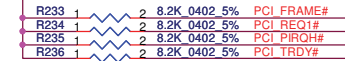
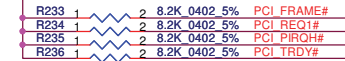
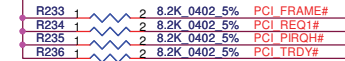
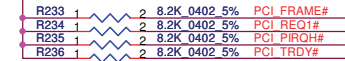
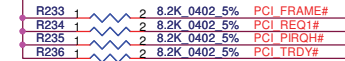
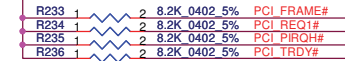
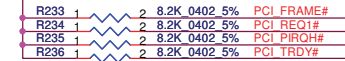
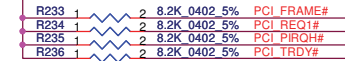
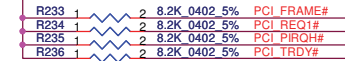
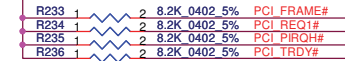
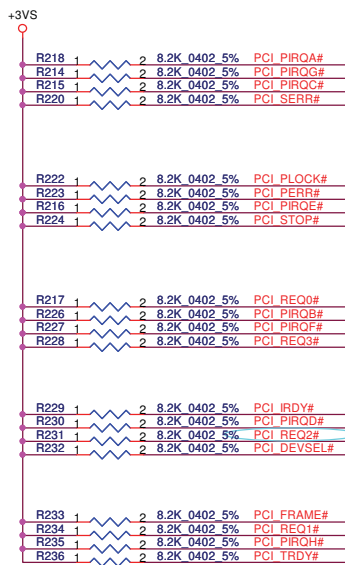


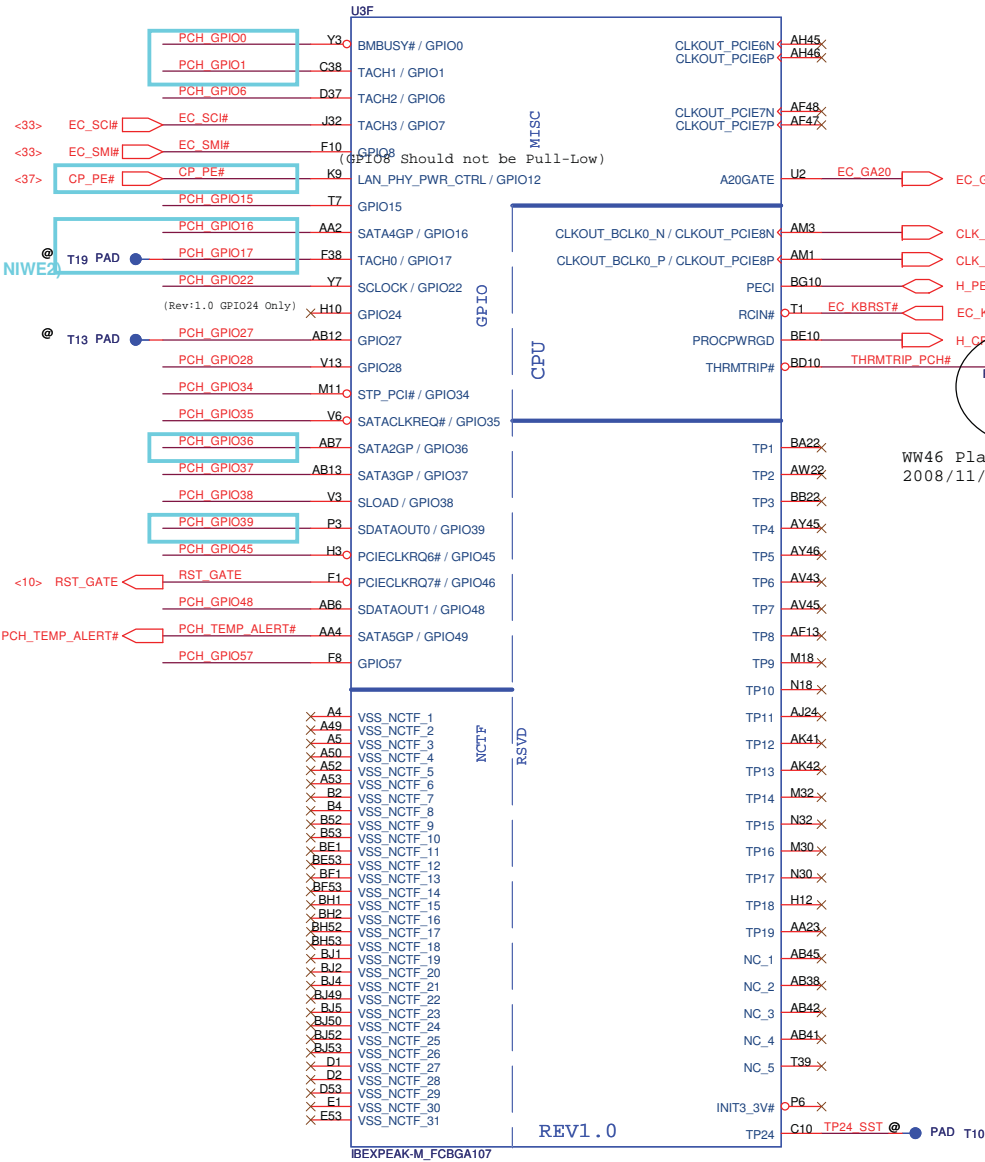
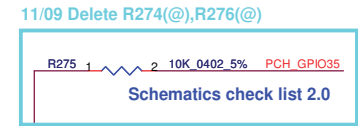
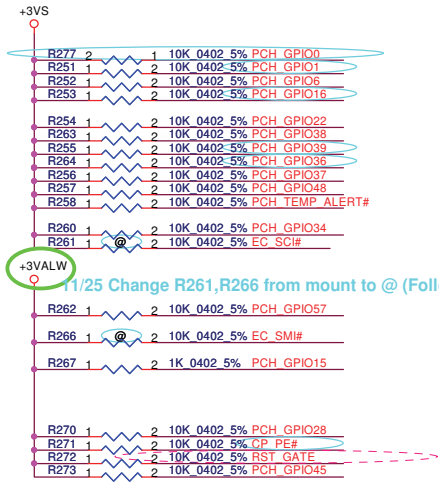
11/06 Change +1.05VS to +1.1VS_VTT

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								Size	Document Number	Rev
									NAU00 M/B LA-6101P Schematics	0
								Date:	Tuesday, March 09, 2010	Sheet

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Size	Custom	Document Number	NAU00 M/B LA-6101P Schematics	Rev	1.0
Date:	Tuesday, March 09, 2010	Sheet	16	of	48





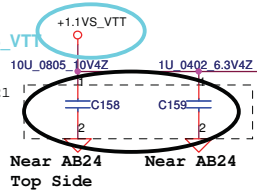


WW46 Platform/Design Updates
2008/11/17 54.9 1% ->56 5%

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										Size	
										Document Number	
										NAU00 M/B LA-6101P Schematics	
										Date:	
										Tuesday, March 09, 2010	
										Sheet	
										18 of 48	

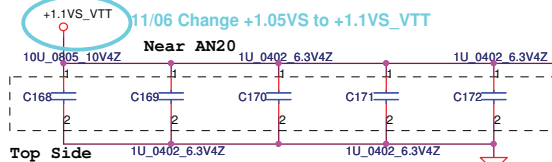
11/06 Change +1.05VS to +1.1VS_VTT

Intel suggest follow CRB 8/21

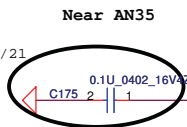


All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

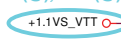
11/09 Delete L6(@),C166(@)



Follow Intel suggestion 8/21

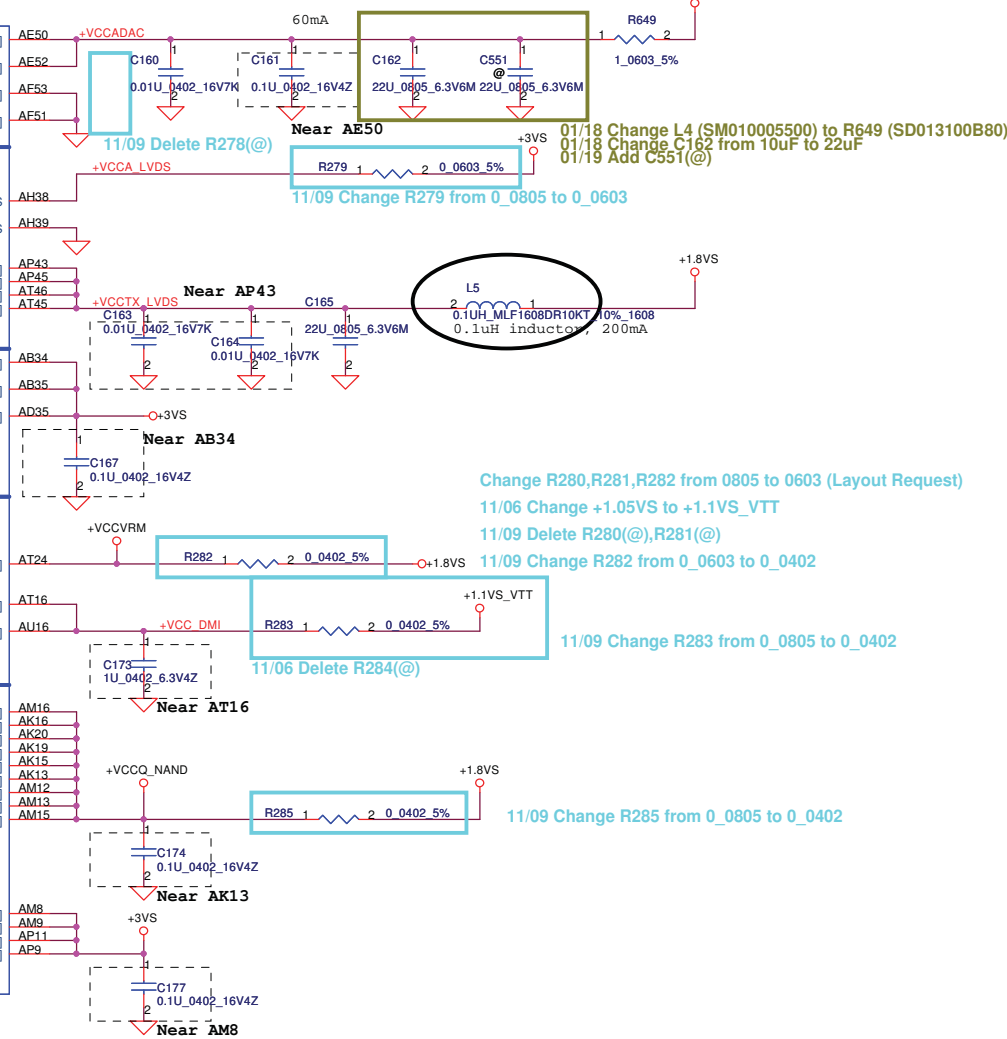
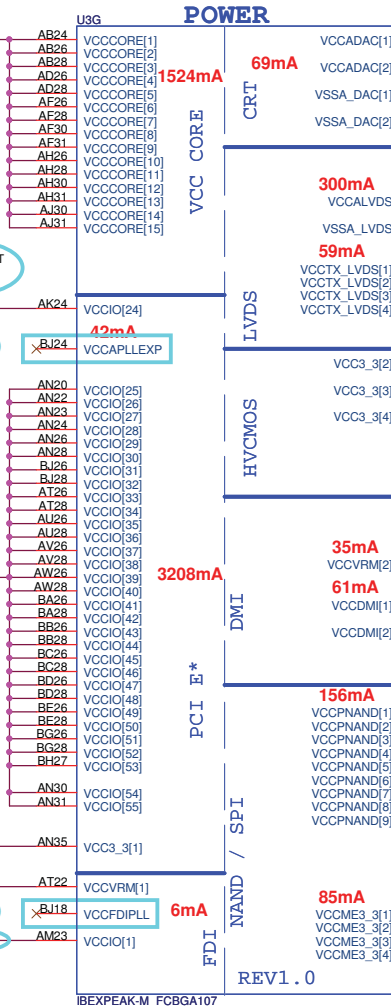


11/09 Delete L7(@),C176(@)



11/06 Change +1.05VS to +1.1VS_VTT

POWER



Change R280,R281,R282 from 0805 to 0603 (Layout Request)

11/06 Change +1.05VS to +1.1VS_VTT

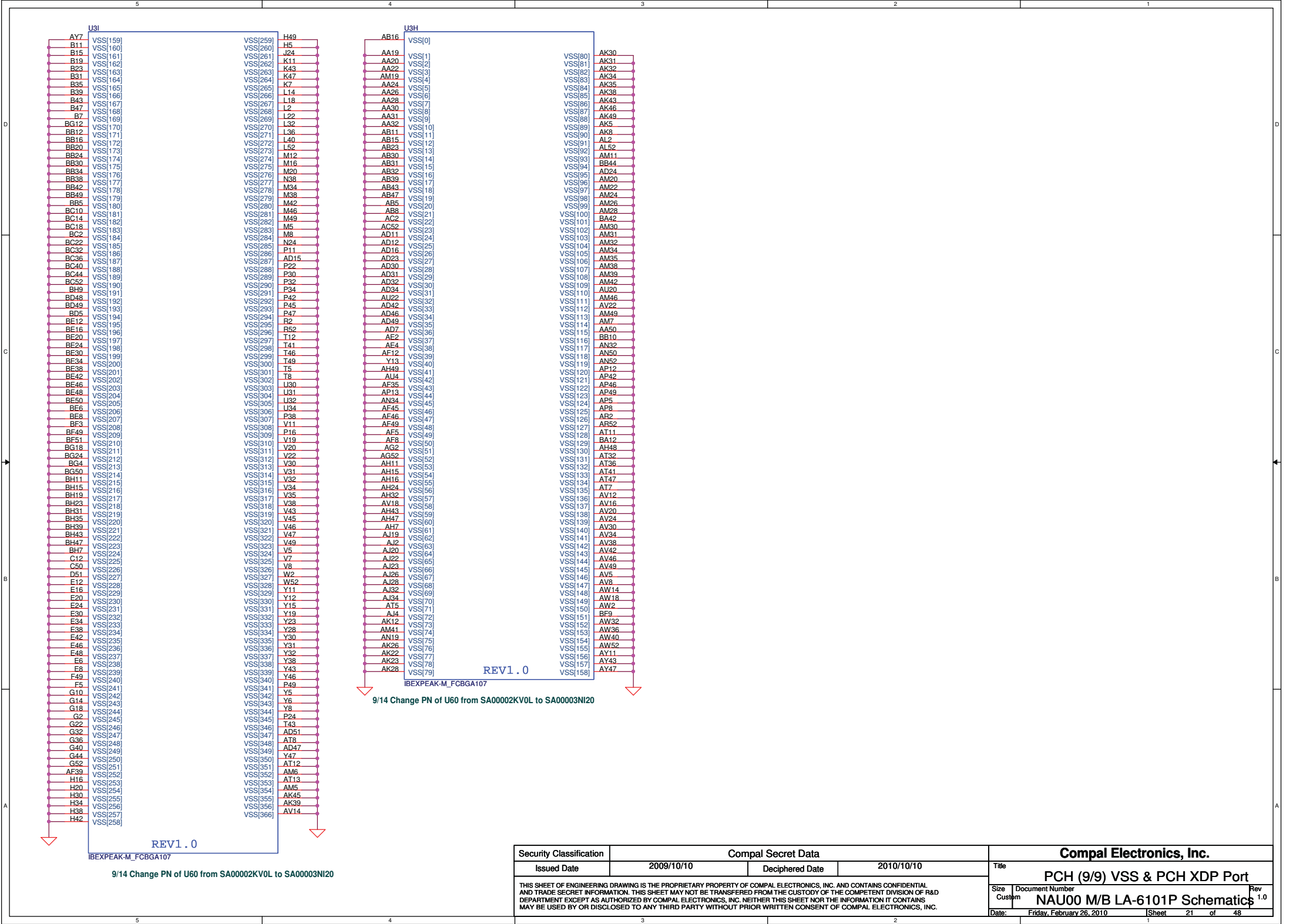
11/09 Delete R280(@),R281(@)

11/09 Change R282 from 0_0603 to 0_0402

11/09 Change R283 from 0_0805 to 0_0402

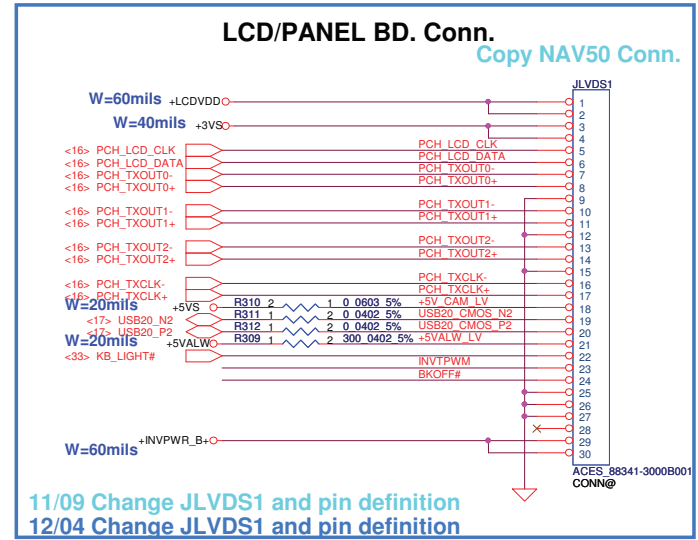
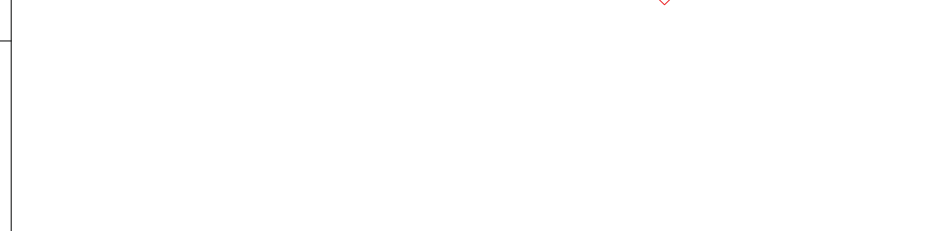
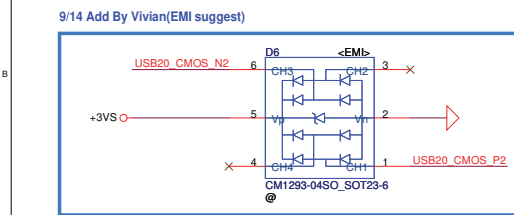
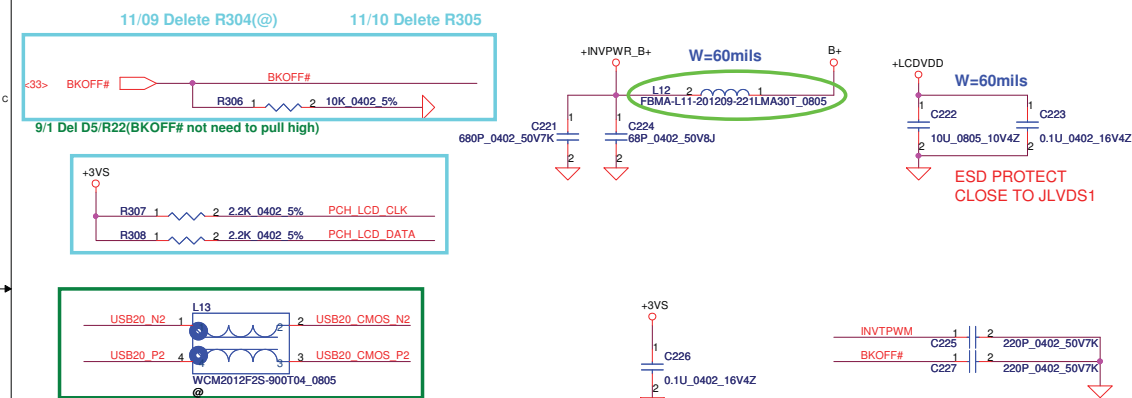
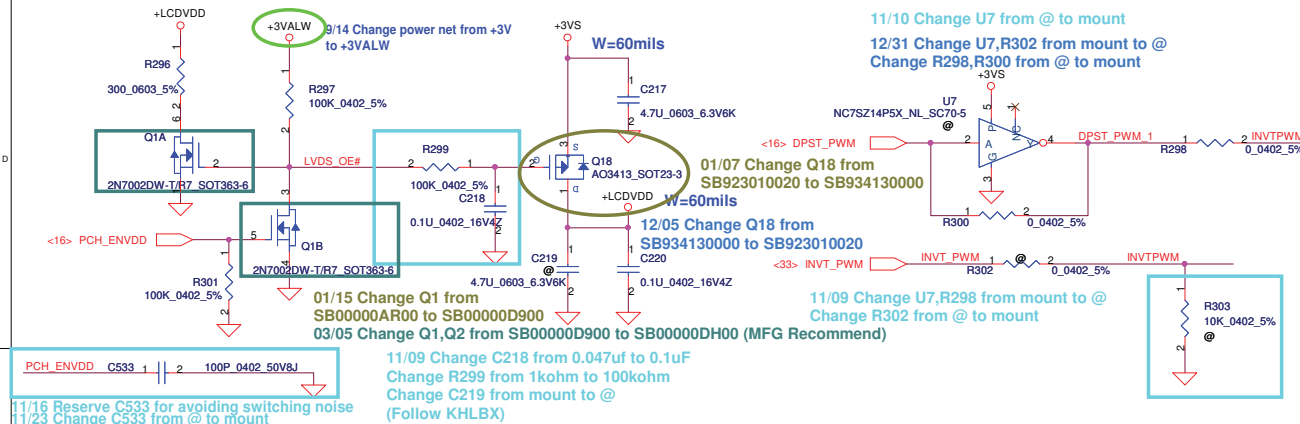
11/09 Change R285 from 0_0805 to 0_0402

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Size	Custom	Document Number	NAU00 M/B LA-6101P Schematics	Rev	0
Date	Friday, February 26, 2010	Sheet	19	of	48



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								PCH (9/9) VSS & PCH XDP Port			
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								Custom	NAU00 M/B LA-6101P Schematics	1.0	
Date:		Friday, February 26, 2010		Sheet		21		of		48	

LCD POWER CIRCUIT

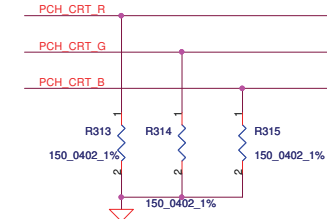


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Issued Date	2009/10/10	Deciphered Date	2010/10/10	Title
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				Document Number
				NAU00 M/B LA-6101P Schematics
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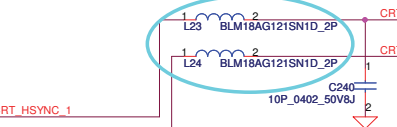
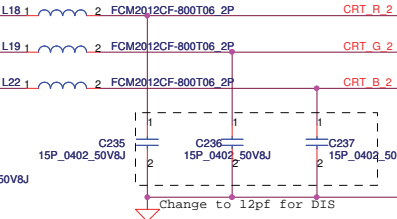
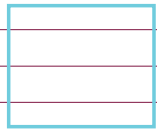
CRT Connector

10/29 Delete L14,L15,L16 (For layout spacing)

<16> PCH_CRT_R
<16> PCH_CRT_G
<16> PCH_CRT_B



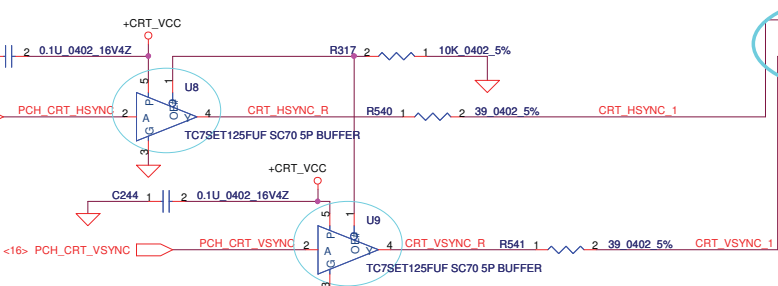
10/29 Delete D8,D9,D10 (For layout spacing)



11/11 Correct L23,L24 footprint



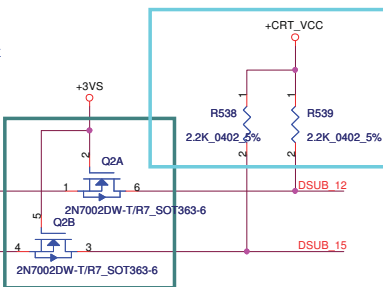
11/03 Change U8,U9 from SA411250130 to SA00000RZ00



PCH DDC PU 2.2K
on Page 17

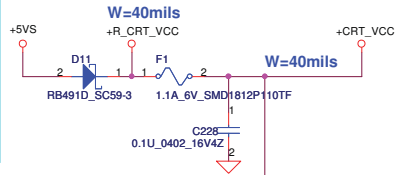
<16> PCH_CRT_DATA

<16> PCH_CRT_CLK

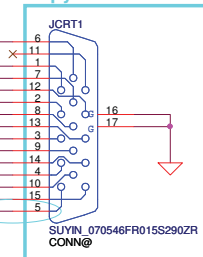


01/15 Change Q2 from SB00000AR00 to SB00000D900
03/05 Change Q1,Q2 from SB00000DH00 to SB00000DH00 (MFG Recommend)

9/10 Change from 2N7002E-T1-E3_SOT23-3 to 2N7002DW-T/R7_SOT363-6
Michael

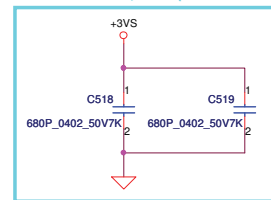


Copy KAV60



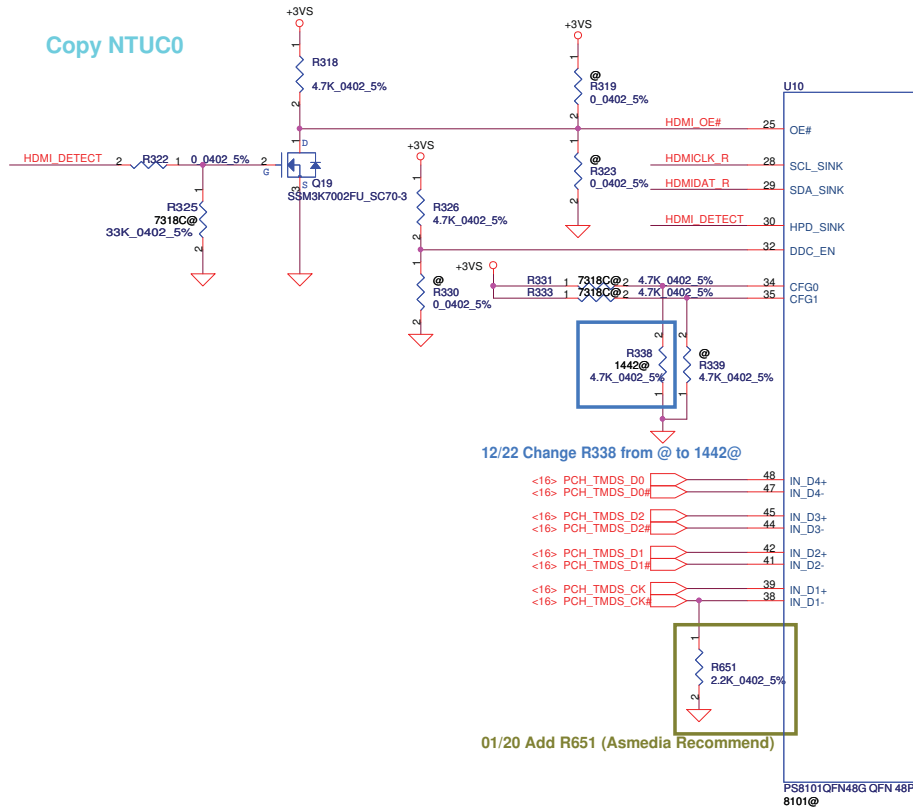
0909 Change JCRT1 symbol from KAVAA

11/10 Add C518,C519 (EMI Recommend)



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					NAU00 M/B LA-6101P Schematics
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Copy NTUC0



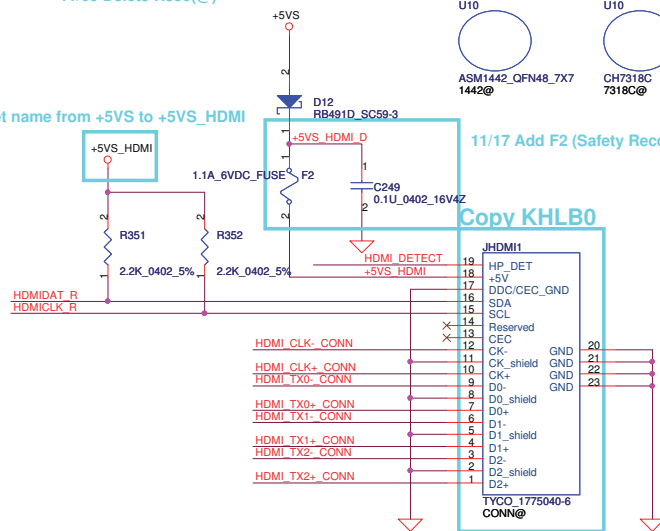
12/22 Change R338 from @ to 1442@

01/20 Add R651 (Asmedia Recommend)

11/09 Delete R350(@)

11/17 Change net name from +5VS to +5VS_HDMI

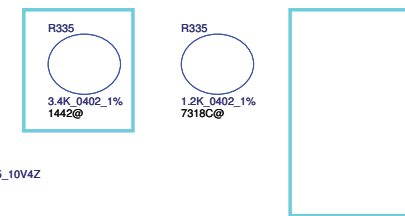
11/17 Add F2 (Safety Recommend)



Copy KHLB0

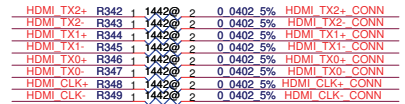
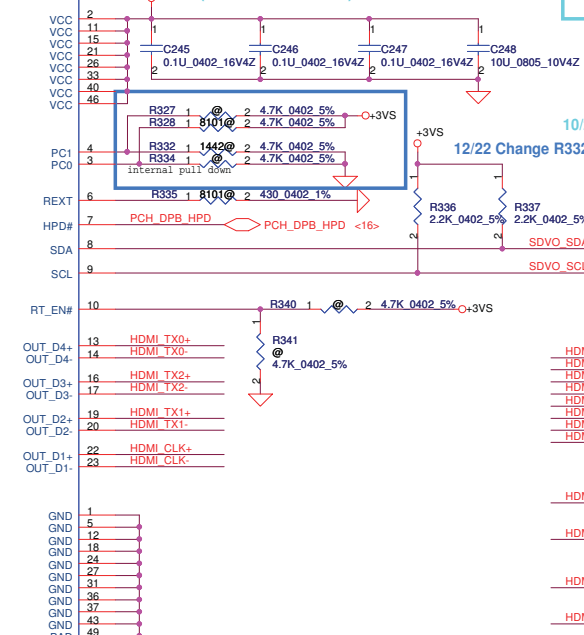
10/22 Change R335(1442@) from 3.3kohm to 3.4kohm (Vendor Recommend)

10/23 Change R327 from 7318C@ from @ Change R332 from @ to 7318C@ (Vendor Recommend)

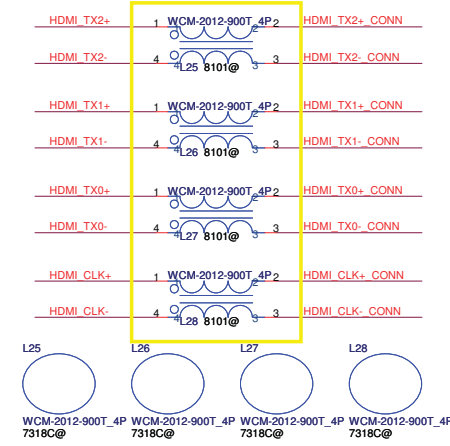


10/23 Delete R324(7318C@), R329(7318C@) for Calpella

12/22 Change R332 from 7318C@ to 1442@



06/25 Mirror L8,L9,L10,L11



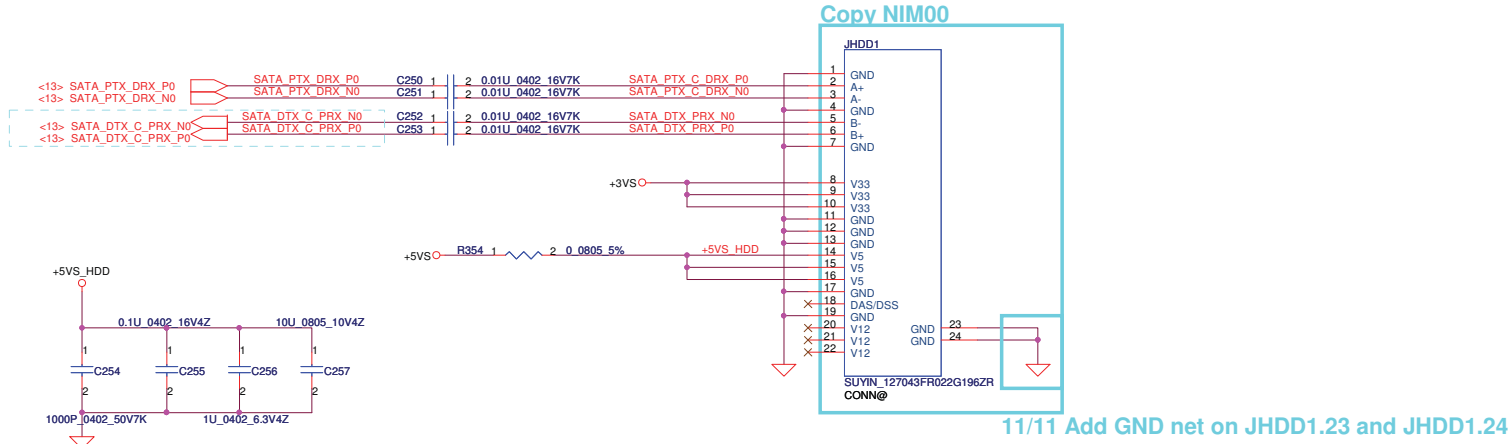
11/09 Delete R353



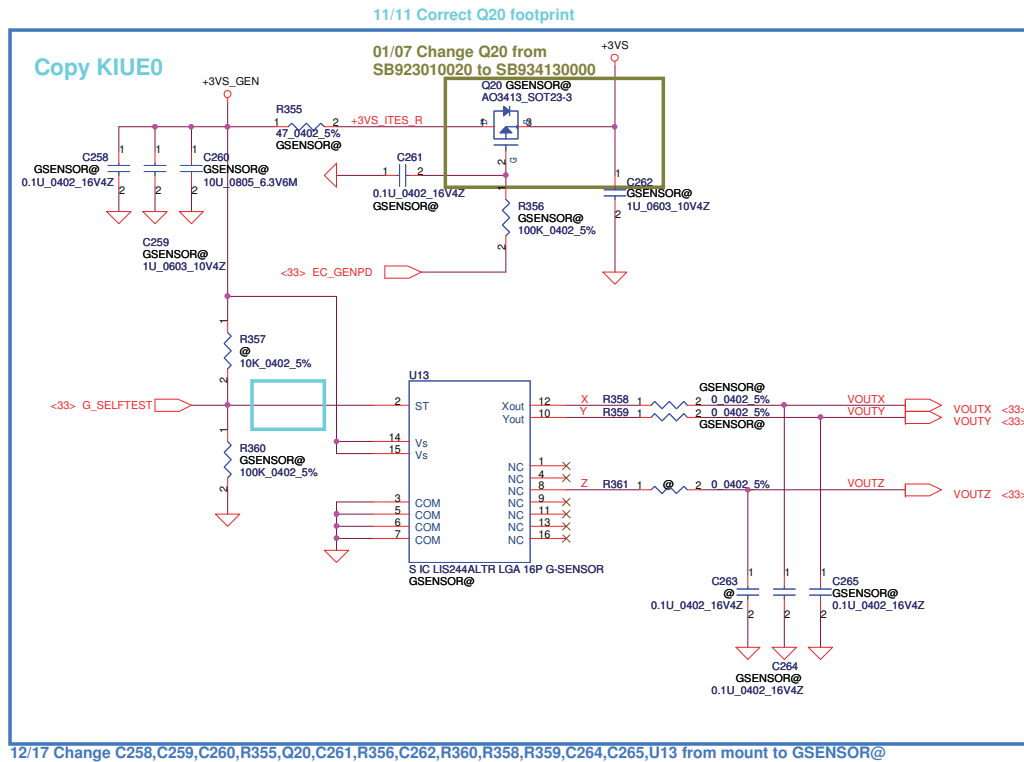
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Size	Document Number	NAU00 M/B LA-6101P Schematics		Rev	1.0
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HDD

SATA HDD Conn.

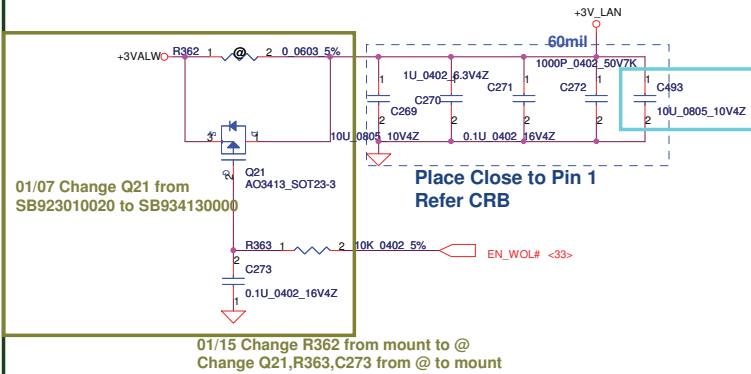


G-Sensor



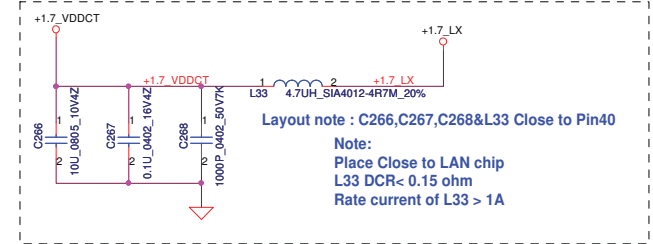
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LAN Power Circuit & Refer NTUC0



01/07 Change Q21 from
SB923010020 to SB934130000

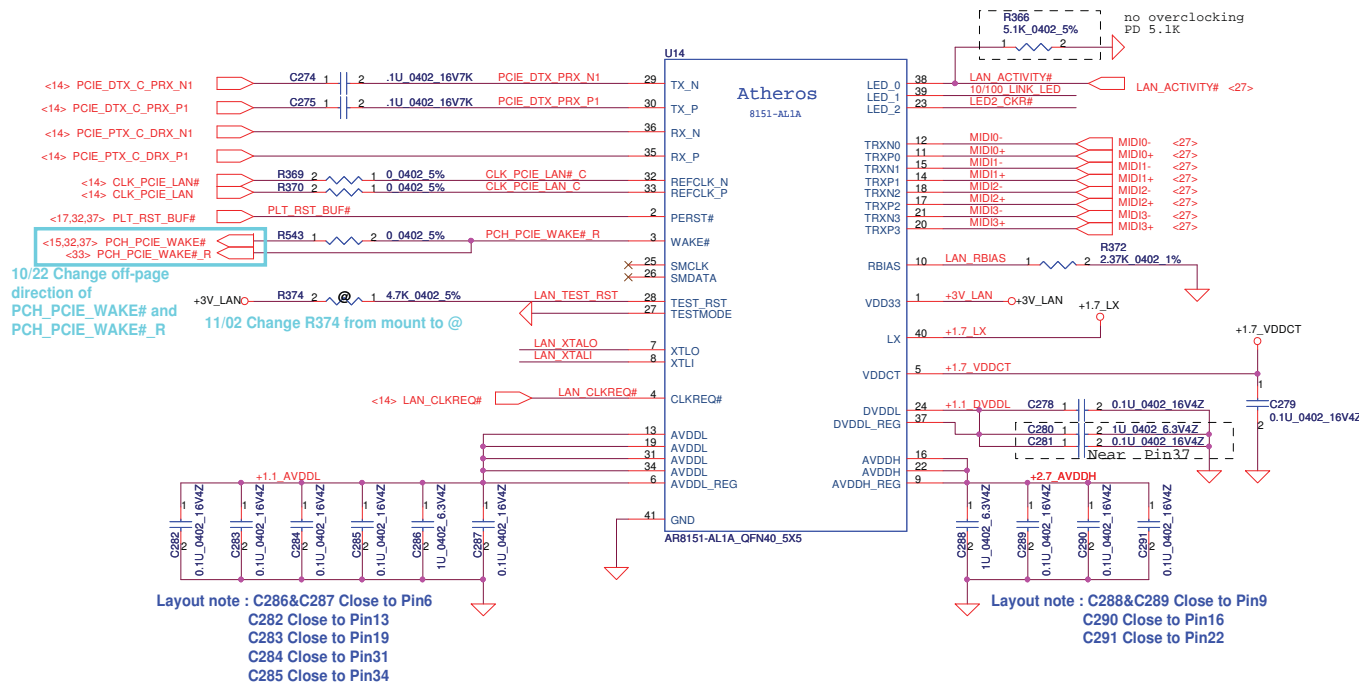
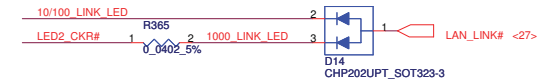
01/15 Change R362 from mount to @
Change Q21,R363,C273 from @ to mount



Layout note : C266,C267,C268&L33 Close to Pin40

Note:
Place Close to LAN chip
L33 DCR< 0.15 ohm
Rate current of L33 > 1A

10/22 Remove R364

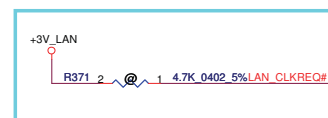


10/22 Change off-page
direction of
PCH_PCIE_WAKE# and
PCH_PCIE_WAKE#_R

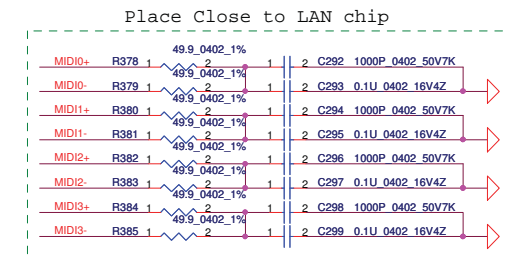
11/02 Change R374 from mount to @

Layout note : C286&C287 Close to Pin6
C282 Close to Pin13
C283 Close to Pin19
C284 Close to Pin31
C285 Close to Pin34

Layout note : C288&C289 Close to Pin9
C290 Close to Pin16
C291 Close to Pin22

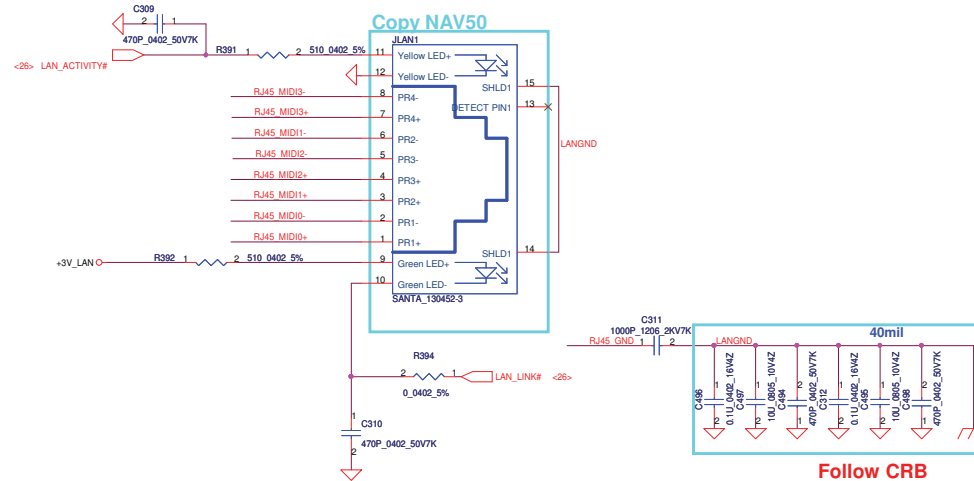
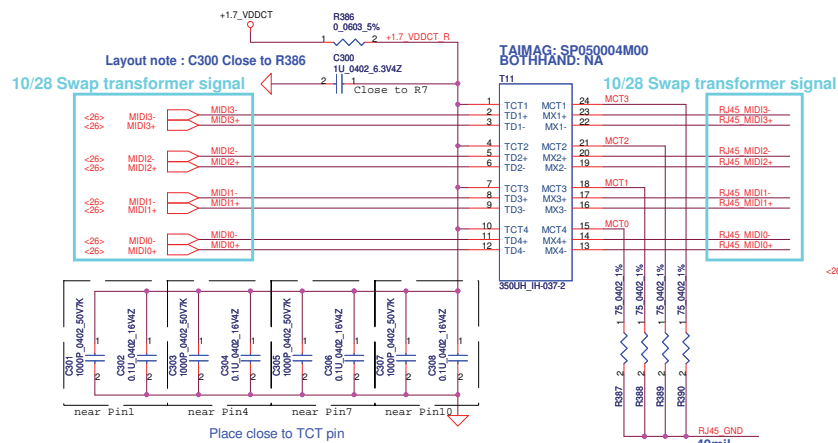


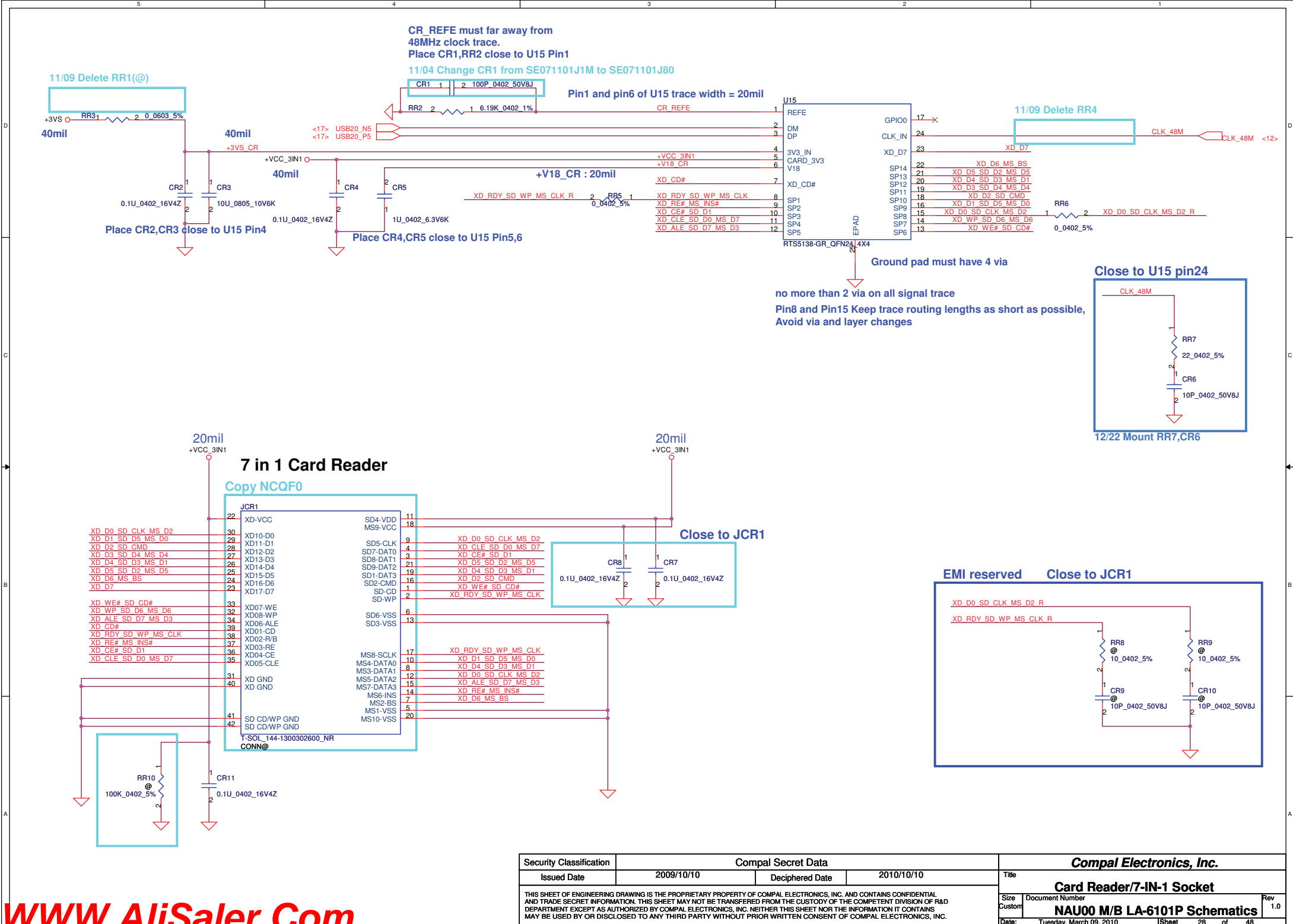
10/22 Change R376 from mount to @
11/02 Change R373 from mount to @
11/02 Delete Q3(@),R375(@),R377(@)
11/09 Delete R373(@),R376(@)



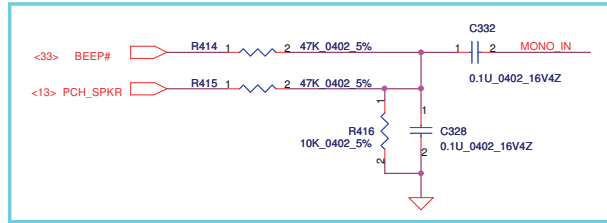
Place Close to LAN chip

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				Custom	NAU00 M/B LA-6101P Schematics	
				Date:	Tuesday, March 09, 2010	

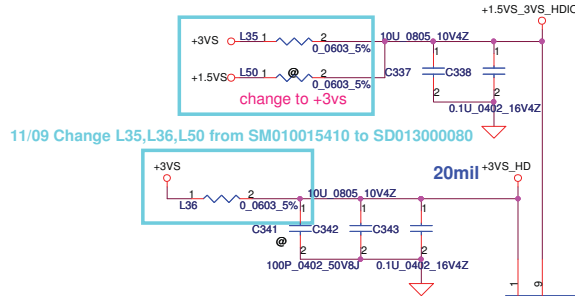
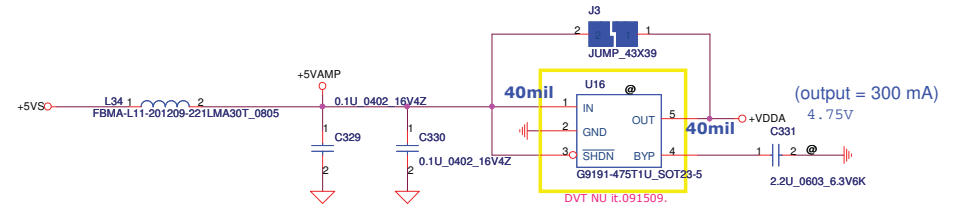




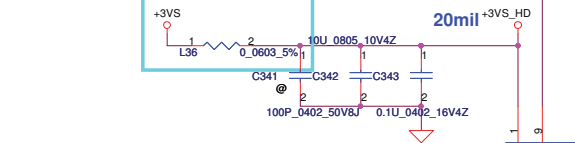
10/29 Follow NTUC0



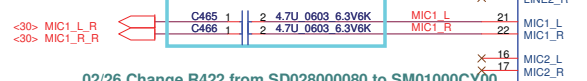
10/29 Delete C333,C334,D15,Q22,R411,R412,R413
Change R414,R415 from 560ohm to 47kohm
Change C332,C328 from 1uF to 0.1uF



11/09 Change L35,L36,L50 from SM010015410 to SD013000080

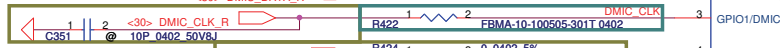


11/10 Change R465,R466 from SE053475Z80 to SE107475M80 (Realtek Recommend)



02/26 Change R422 from SD028000080 to SM01000CY00

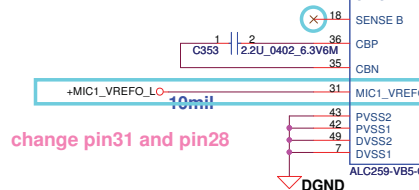
01/07 Change C351.2 from R422.2 to R422.1



01/07 Add R648(@) to +HD_AVDD (Realtek Recommend)

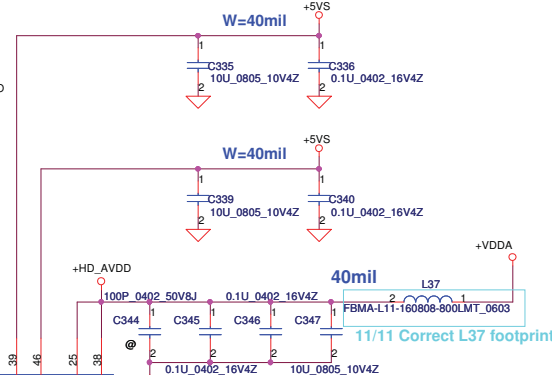


10/30 Change C352 GND from AGND to GND

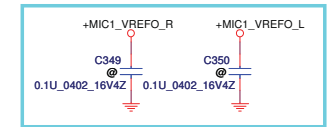
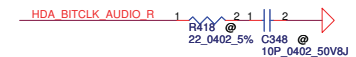


change pin31 and pin28

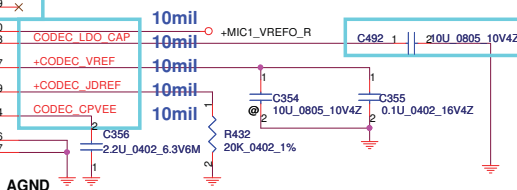
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 32, 33)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 48)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 20)
	5.1K	PORT-H (PIN 47)



11/11 Correct L37 footprint



11/05 Add net name : CODEC_LDO_CAP,+CODEC_VREF,+CODEC_JDREF,CODEC_CPVEE



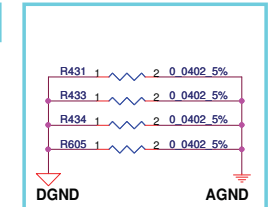
10/21 Change U17 to SA00003QR00 Symbol

03/04 Change U17 from SA00003QR00 to SA00003QR10

11/02 Change R429,R430,R431,R433,R434,R605 from 0_0603 to 0_0402 (Layout Spacing)

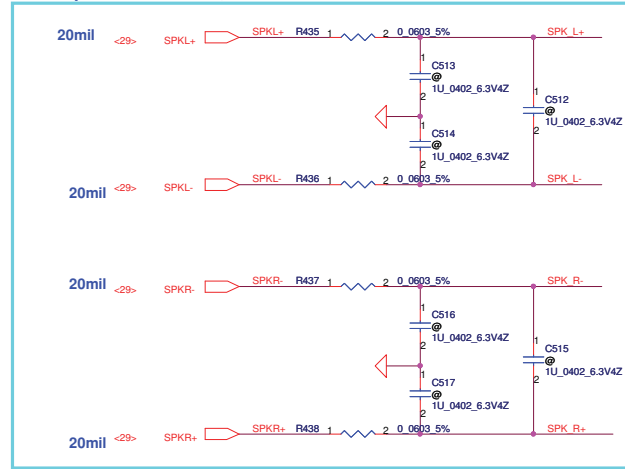
11/17 Delete R429,R430

DGND To AGND Bypass

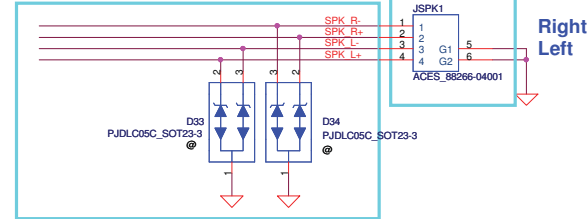


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						Size	Document Number		Rev
						Custom	NXXXX M/B LA-6101P Schematics		1.0
						Date:	Tuesday, March 09, 2010		Sheet 29 of 48

11/11 Change R435~R438 from SM010012010 to SD013000080
 11/10 Add C512~C517(@) for EMI (Follow Realtek CRB)
 Please place R435~R438,C512~C517 close to U17



Int. Speaker Conn.

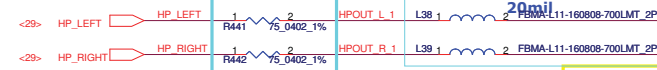


11/18 Change the pin definition of JSPK1 (Audio Recommend)
 11/18 Swap D33

Copy KTV00

Right
Left

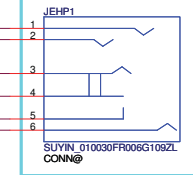
10/29 Change R441,R442 from 56ohm to 75ohm (Follow Realtek CRB)



11/11 Correct L38,L39,L40,L41 footprint

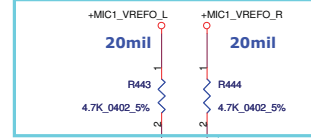
Headphone Out

Copy NIUR1



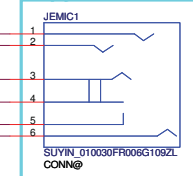
01/07 Change GND to GNDA

10/29 Short D18,D19 (Follow Realtek CRB)
 10/29 Change R443,R444 location



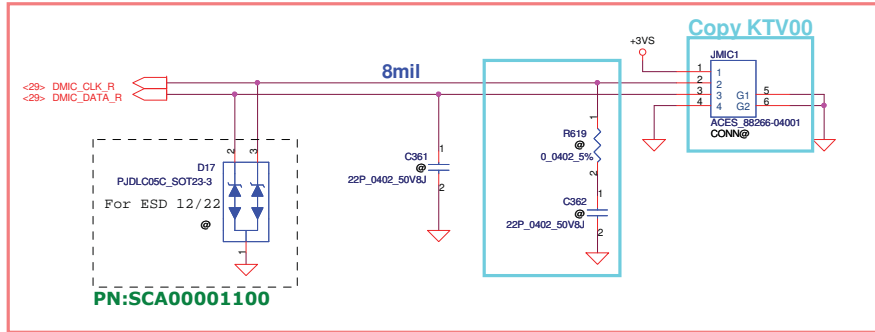
MIC JACK

Copy NIUR1



11/11 Correct D20 footprint

01/07 Change GND to GNDA



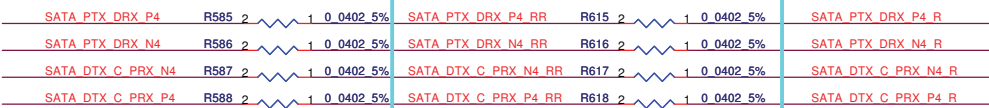
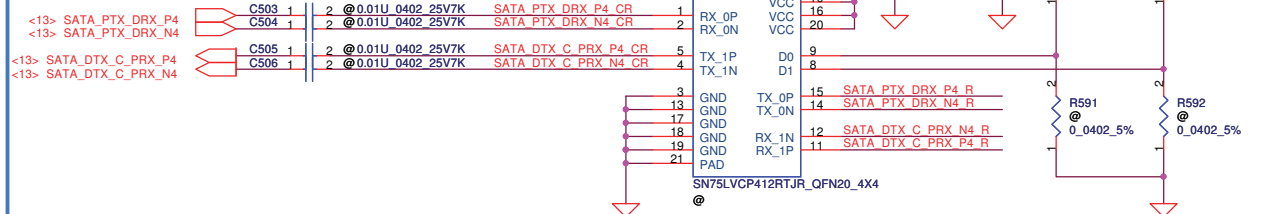
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Issued Date	2009/10/10	Deciphered Date	2010/10/10	Title
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				Customer NXXXX M/B LA-6101P Schematics
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eSATA

10/22 Add R614, change R590,R589 from 0ohm to 4.7kohm (Vendor Recommend)
12/22 Change U32,C490,C491,C503~C506,R589,R590,R614 from mount to @

Copy NITU1

10/23 Add C503~C506



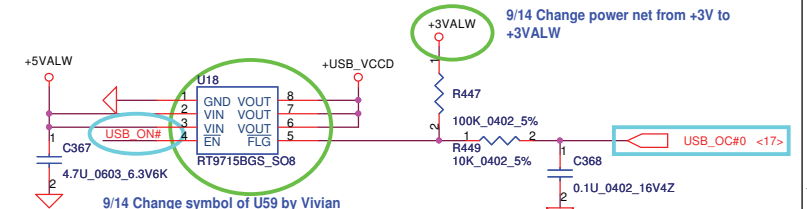
On opposite side of U32

10/23 Add R615~R618

12/22 Change R585~R588,R615~R618 from @ to mount

TI:D0 D1			SN75LVCP412	
EN	BA	BB	CHANNEL 0	CHANNEL 1
0	X	X	Low-power	Low-power
1	0	0	0dB	0dB
1	1	0	2.5dB pre-emphasis	0dB
1	0	1	0dB	2.5dB pre-emphasis
1	1	1	2.5dB pre-emphasis	2.5dB pre-emphasis

(Default)

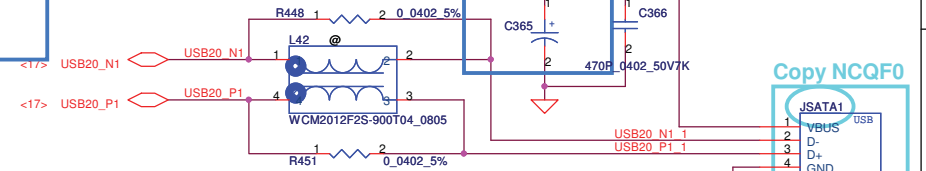


9/14 Change symbol of U59 by Vivian

11/25 Change L42 from @ to mount
Change R451,R448 from mount to @
(EMI Recommend)

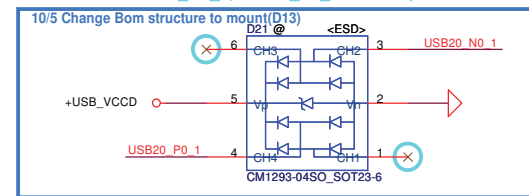
12/27 Change C365 from SGA00002N80 to SGA00001E00

12/22 Change L42 from mount to @
Change R451,R448 from @ to mount
(EMI Recommend)

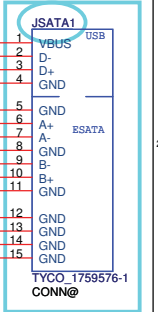


11/09 Change D22 from mount to @

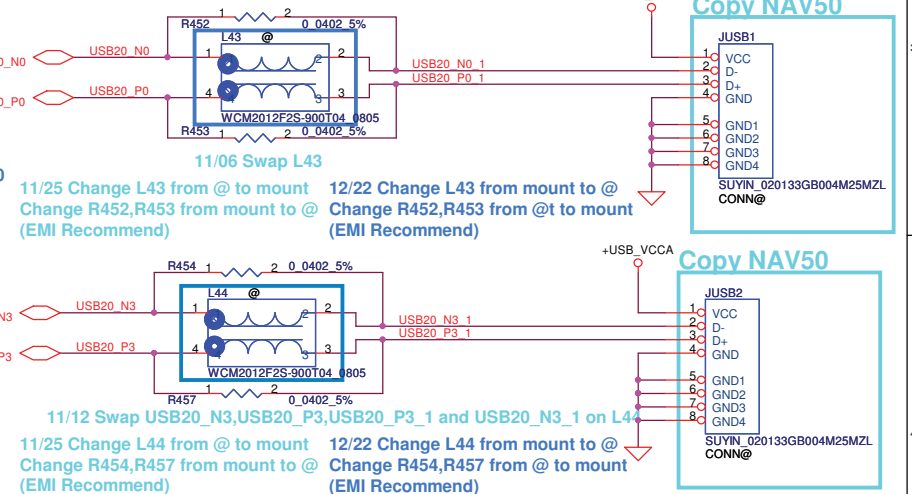
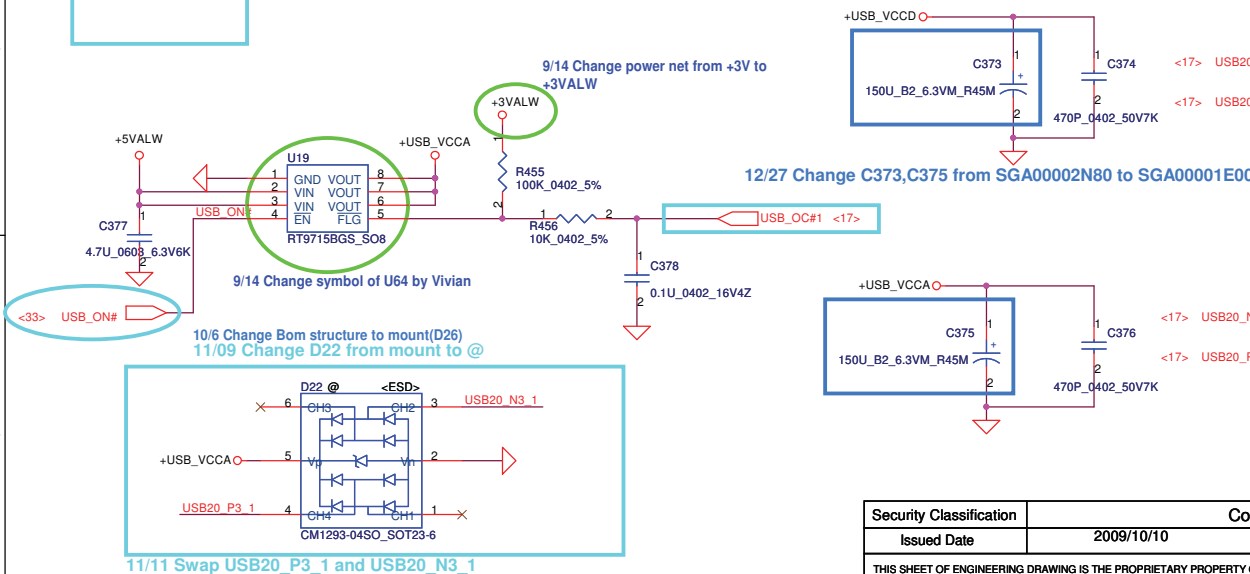
11/05 Delete USB20_N1_1,USB20_P1_1 on D21 (ESD Recommend)



Copy NCQF0



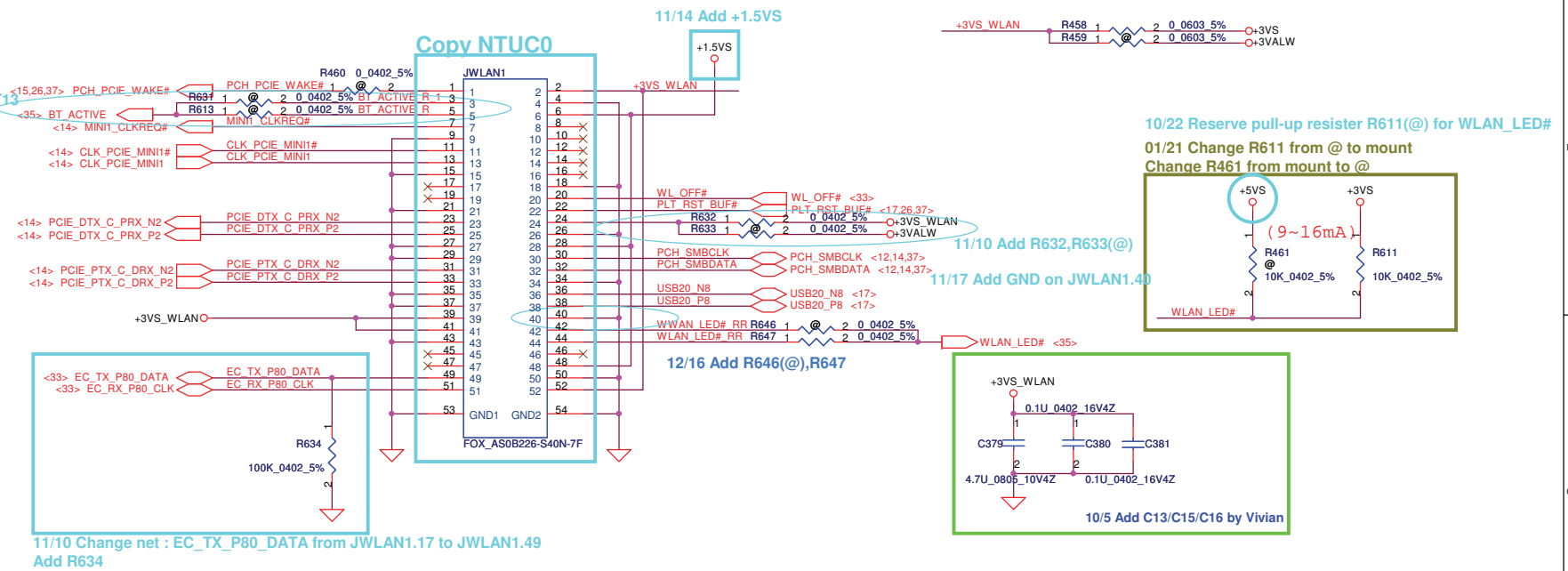
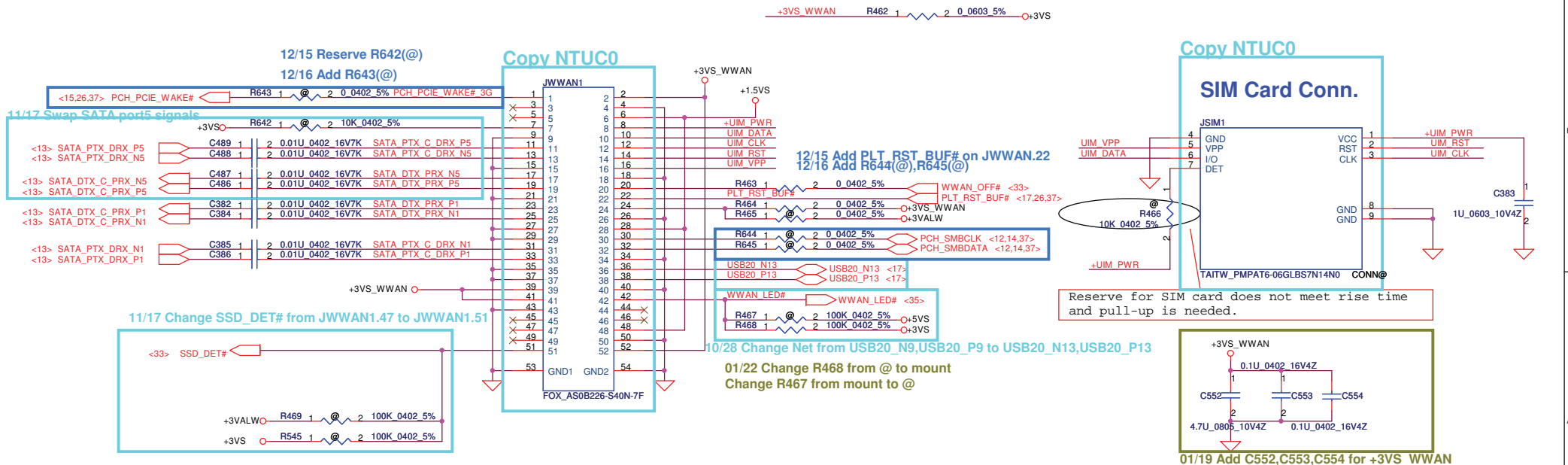
USB Port



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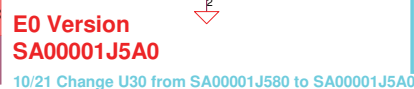
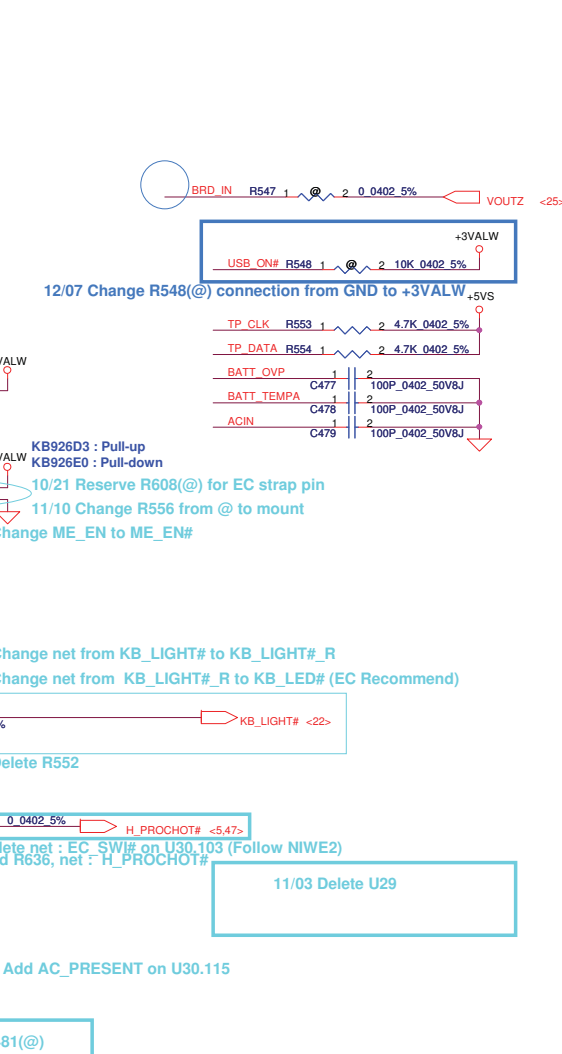
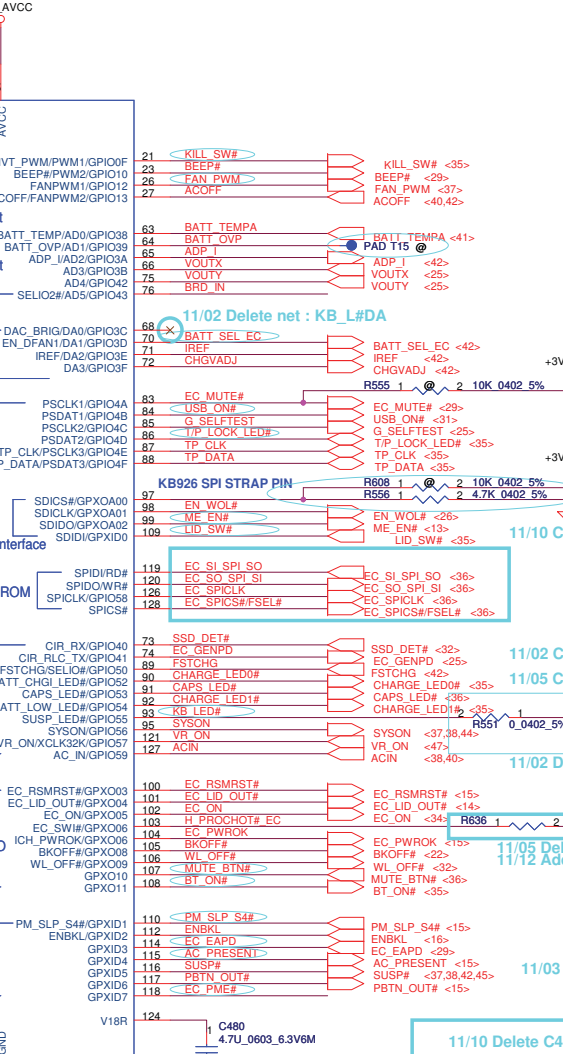
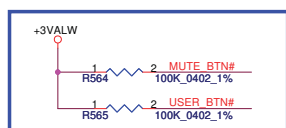
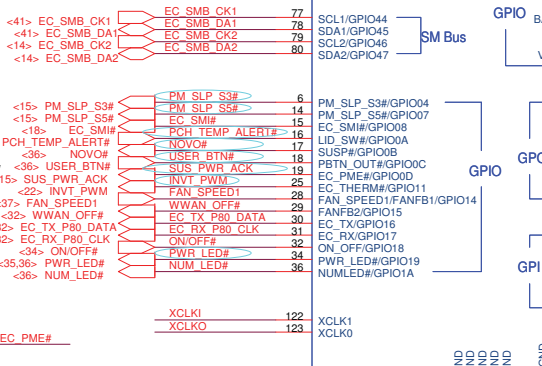
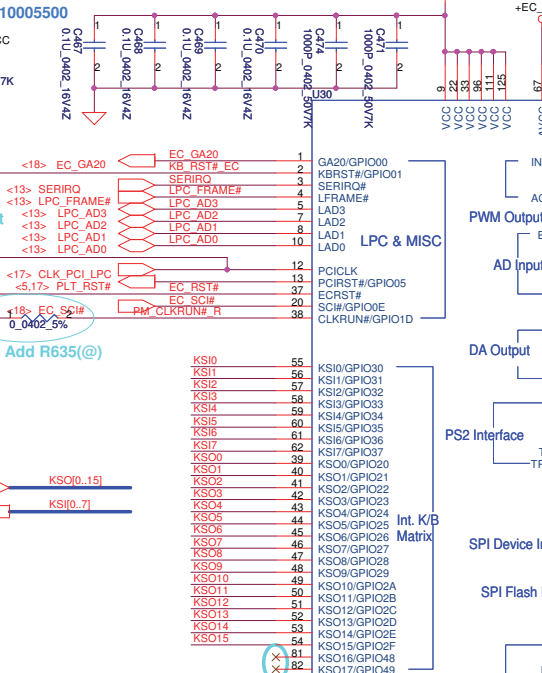
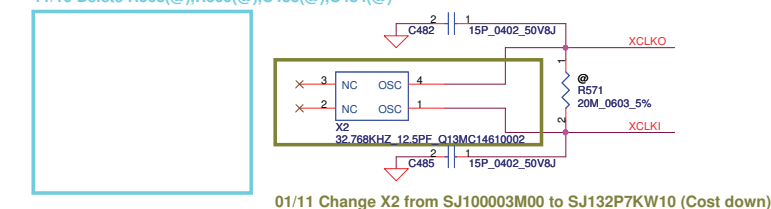
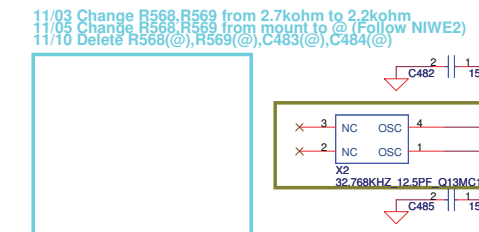
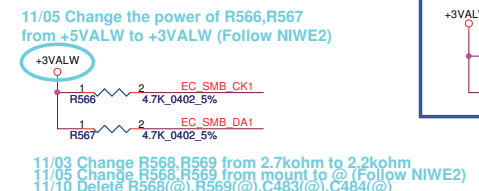
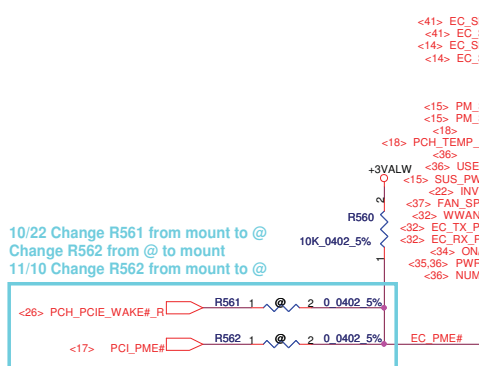
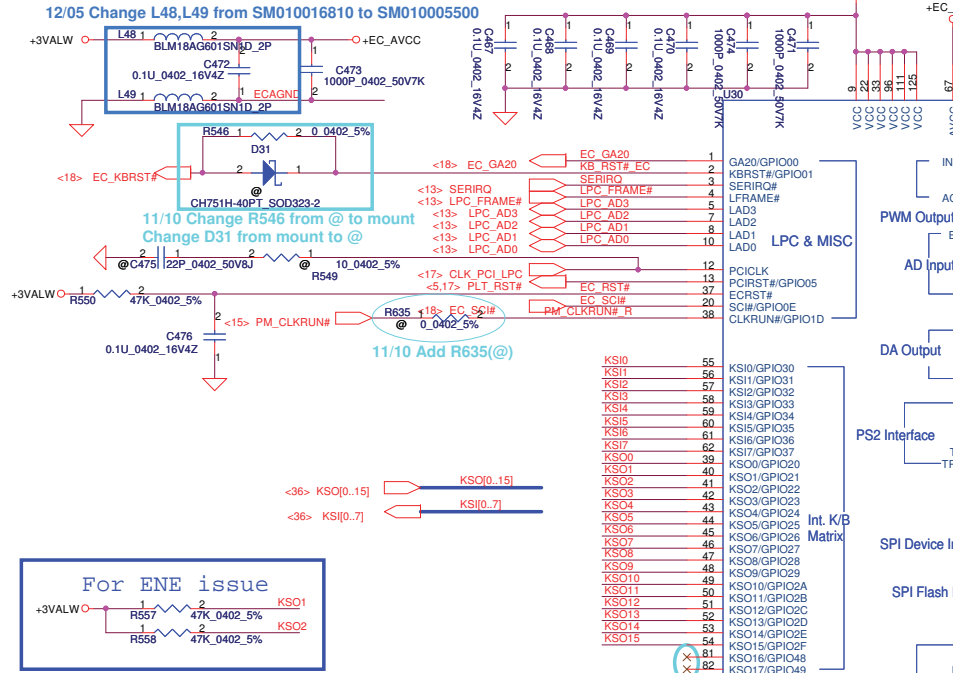
WLAN

10/22 Add Net : BT_ACTIVE and R613, Delete T13
11/10 Add R631(@)

**WWAN**

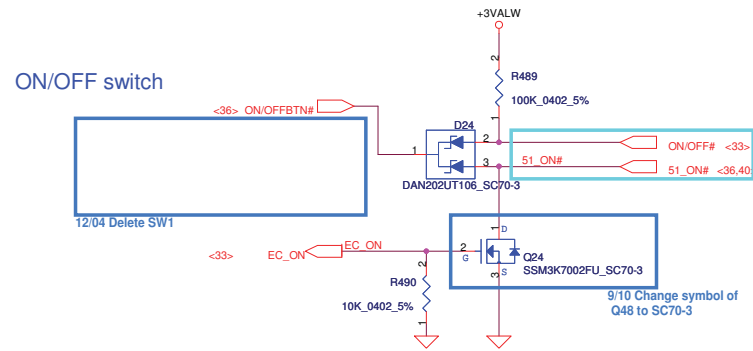
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12/05 Change L48,L49 from SM010016810 to SM010005500



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				Customer	NAU00 M/B LA-6101P Schematics
				Date	Tuesday, March 09, 2010 1:50 PM

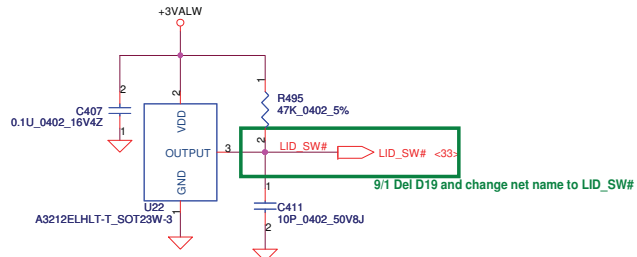
Power Button



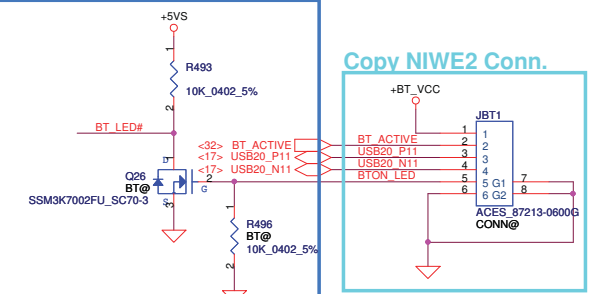
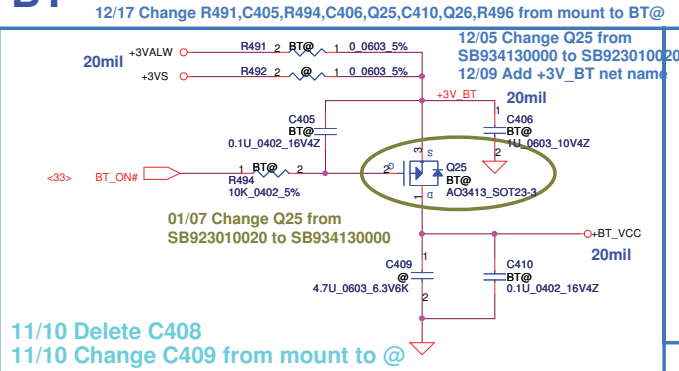
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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Lid Switch

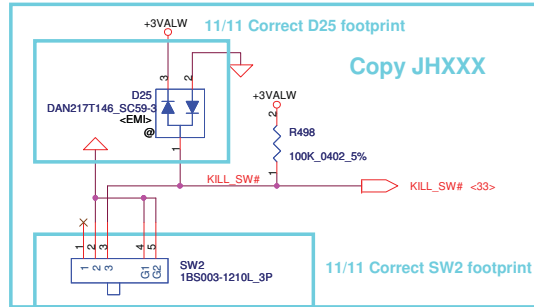
(Hall Effect Switch)



BT

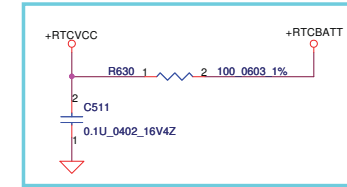


KILL Switch

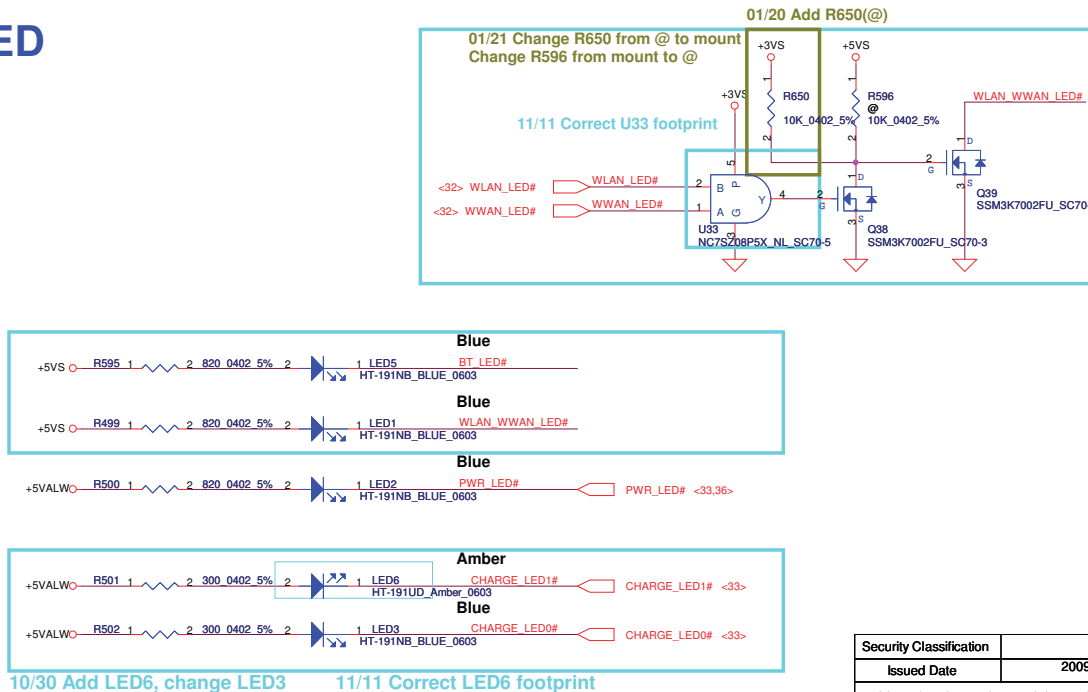


RTC

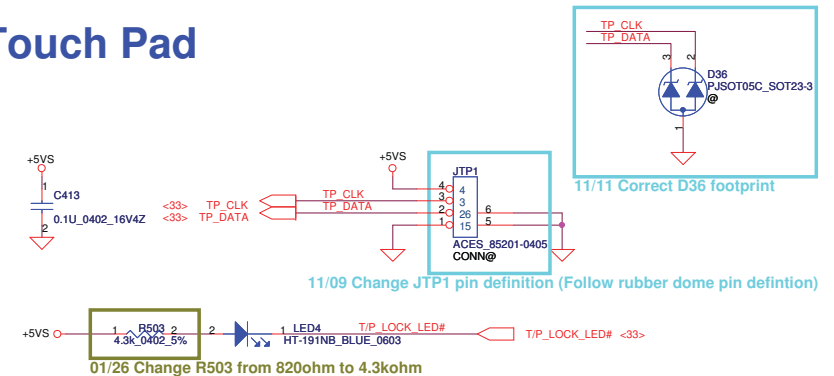
11/10 Delete D26,C412,R497, Add R630,C511 (Follow NIWE2)



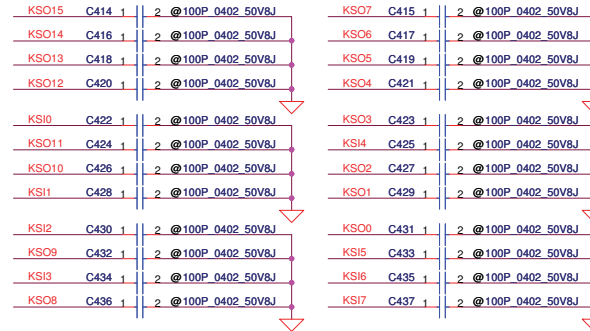
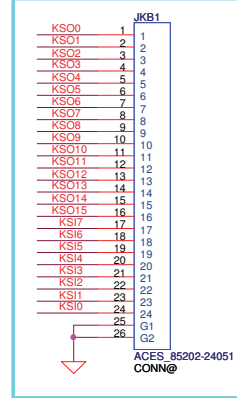
LED



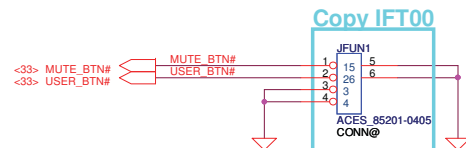
Touch Pad



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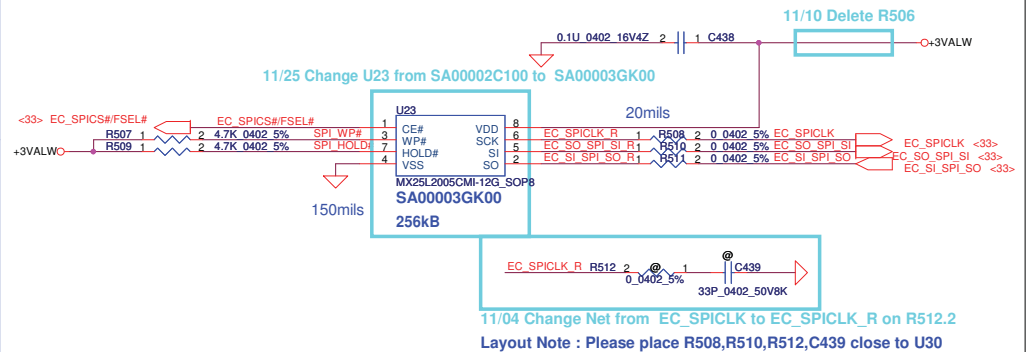
FingerPrint/B Conn.



Copy KSW01



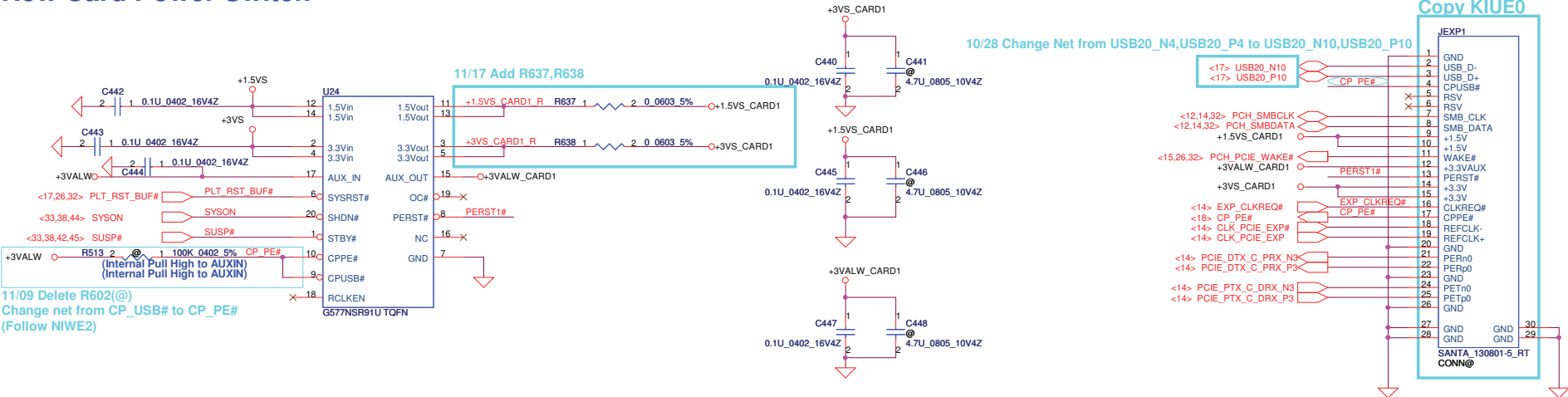
EC SPI ROM



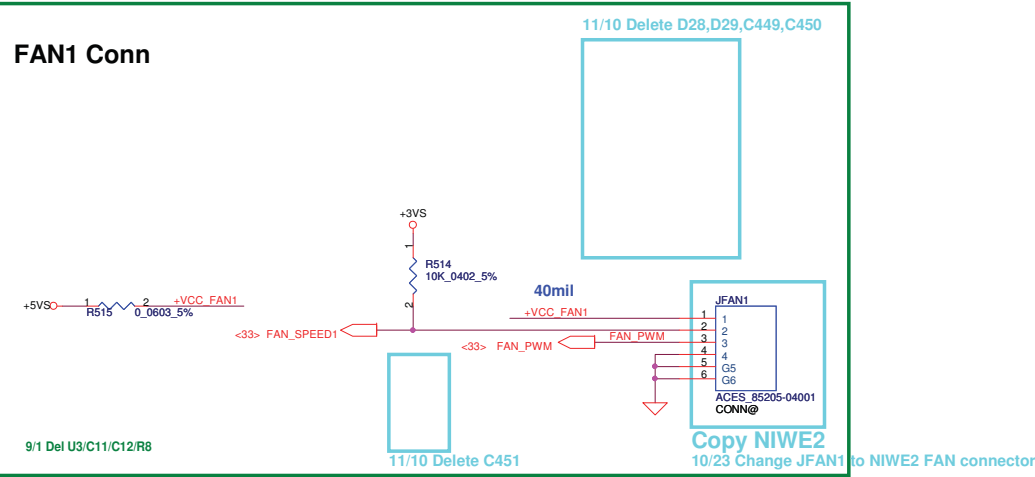
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				Date	Transferred Month/0 Year

New Card Socket

New Card Power Switch



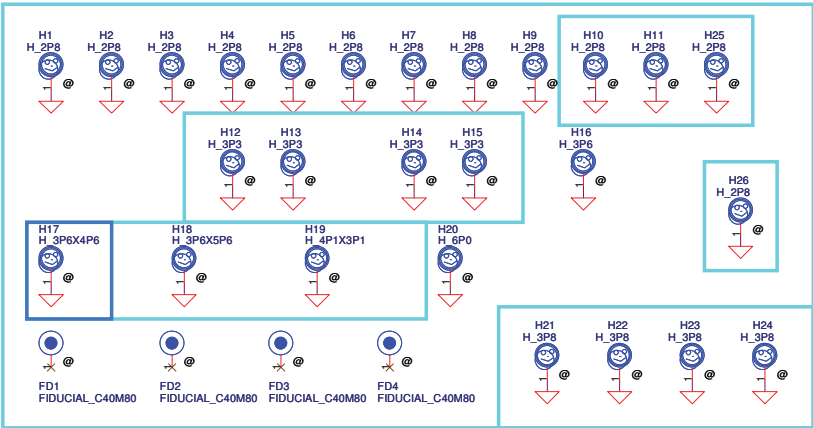
FAN1 Conn



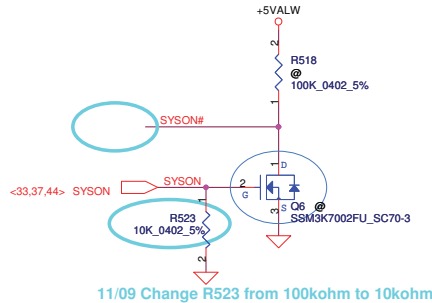
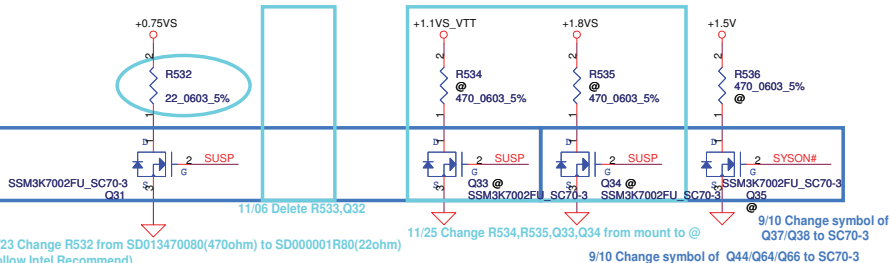
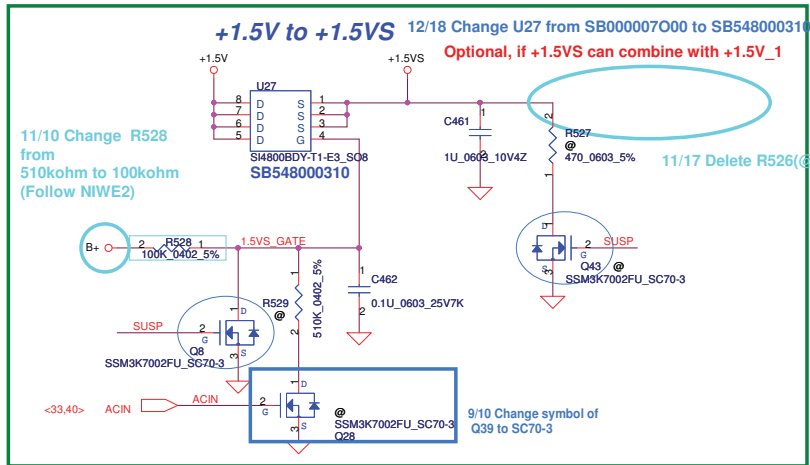
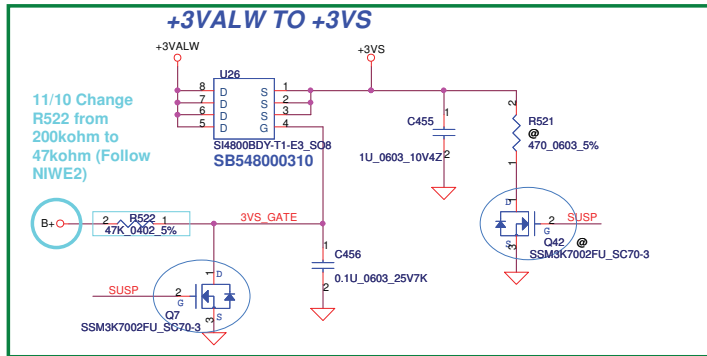
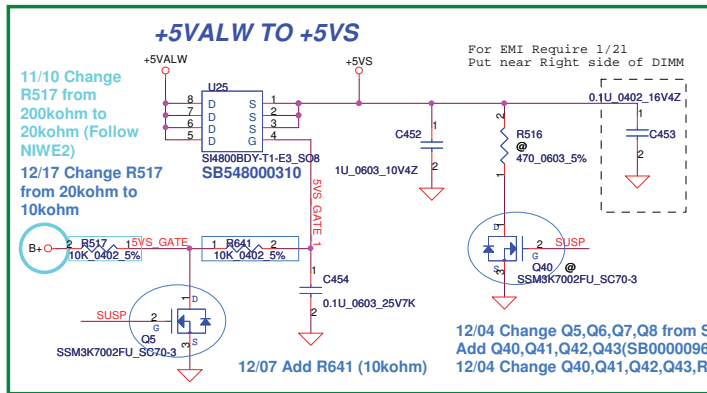
12/10 Change H17 from H_3P6X5P6 to H_3P6X4P6

11/14 Add H26 H_2P8

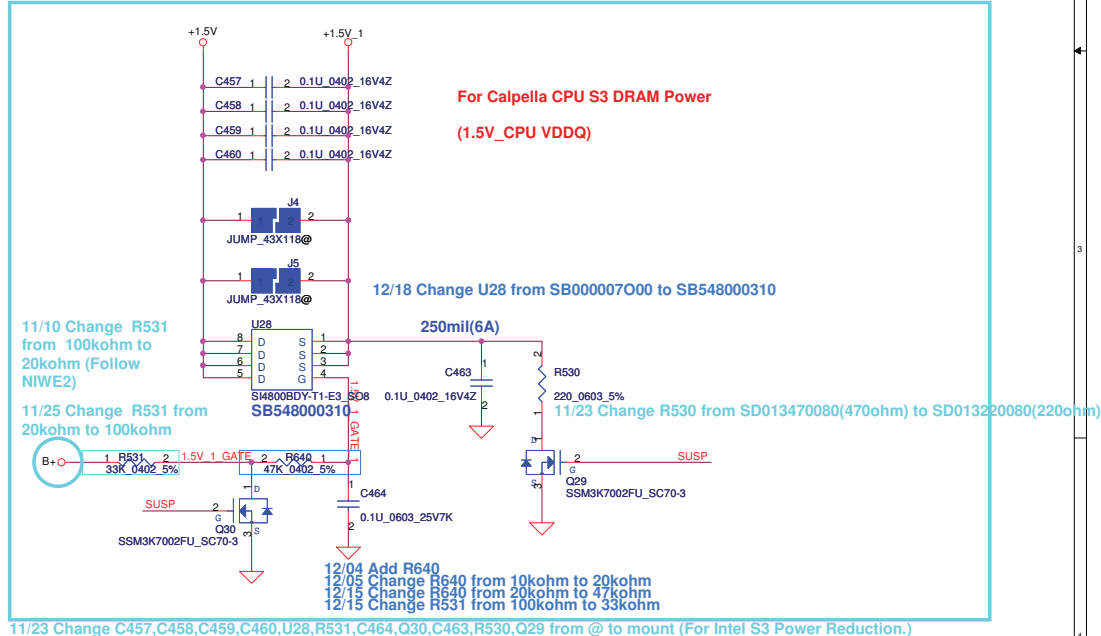
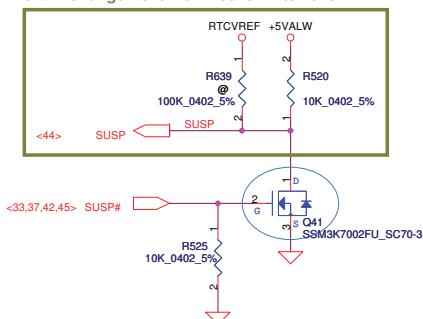
11/11 Change H12-H15 to H_3P3



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Size B	Document Number	NAU00 M/B LA-6101P Schematics		Rev	1.0
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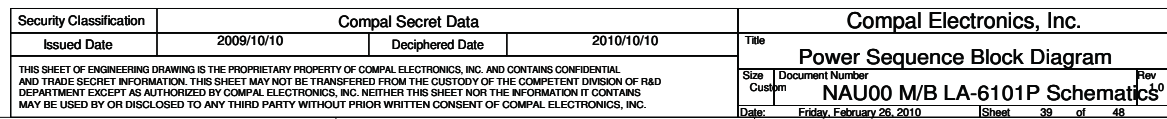


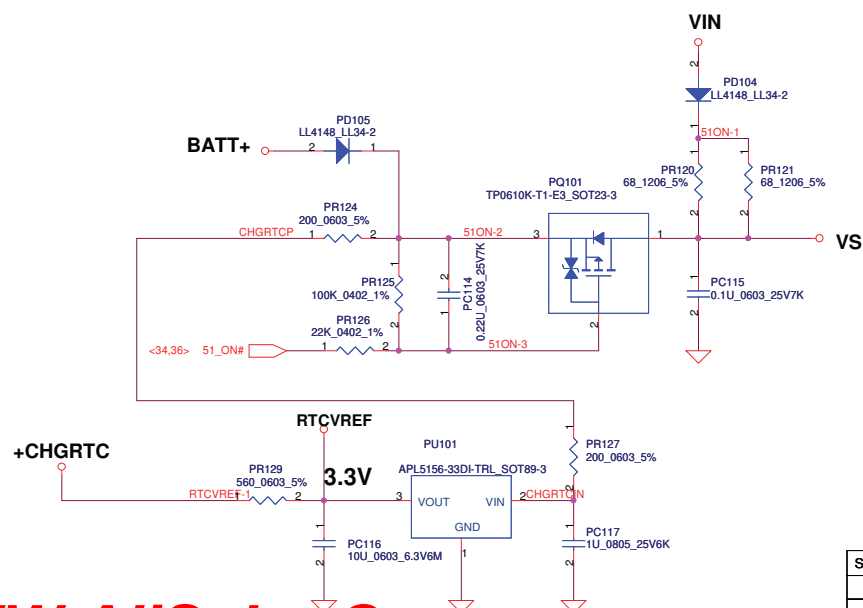
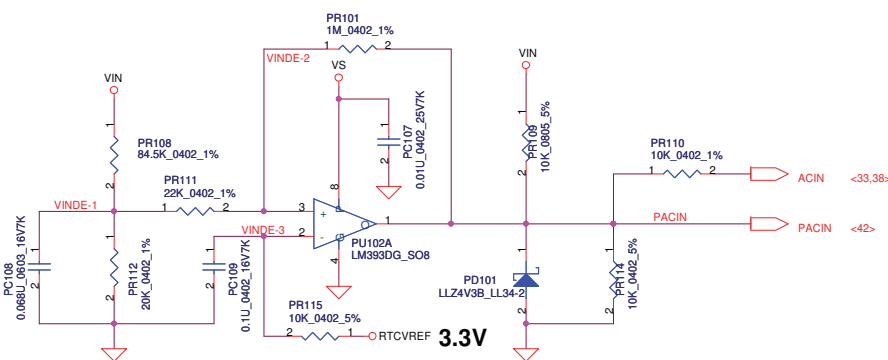
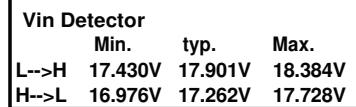
12/04 Add R639, Change R520 from mount to @
01/21 Change R520 from @ to mount
Change R639 from mount to @
01/21 Change R520 from 100kohm to 10kohm



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				Size B	Document Number			Rev	1.0
				NAU00 M/B LA-6101P Schematics					
				Date:	Tuesday, March 09, 2010		Sheet	38 of 48	

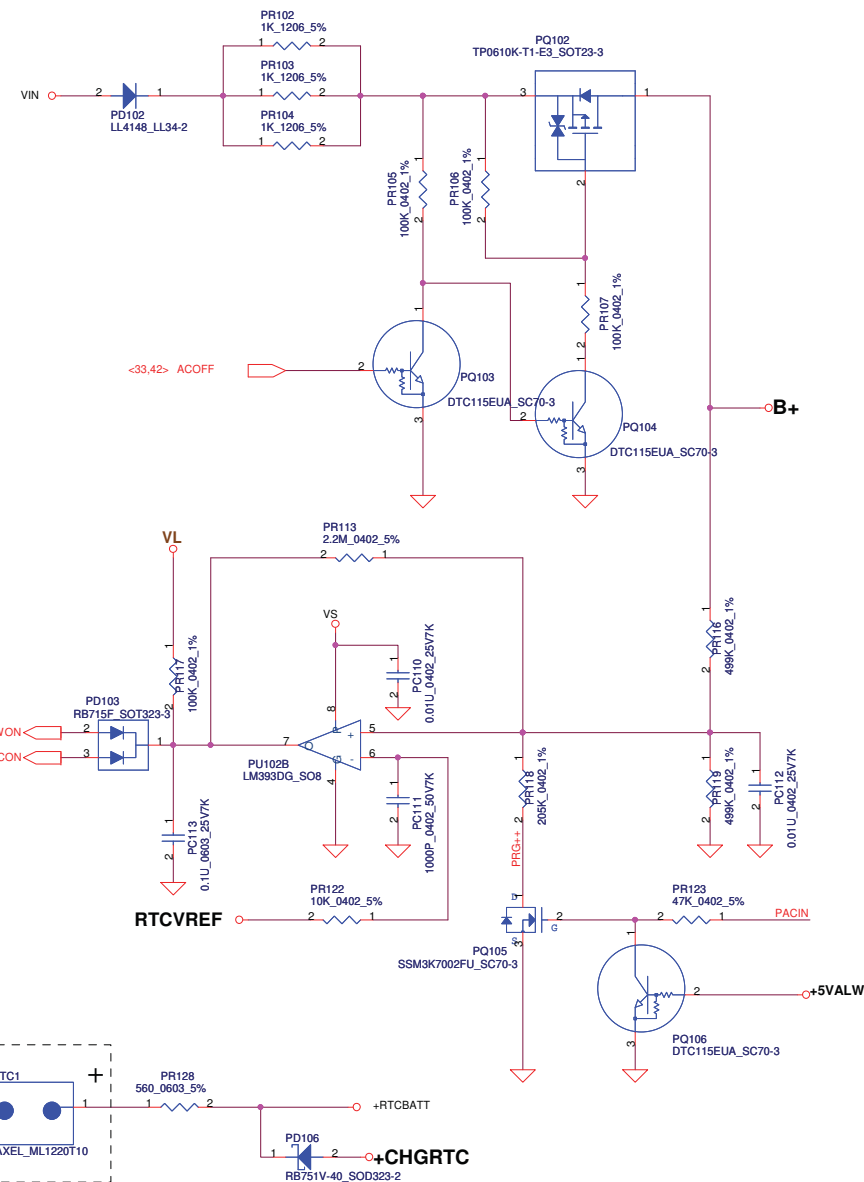
MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*





	Precharge detector		
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

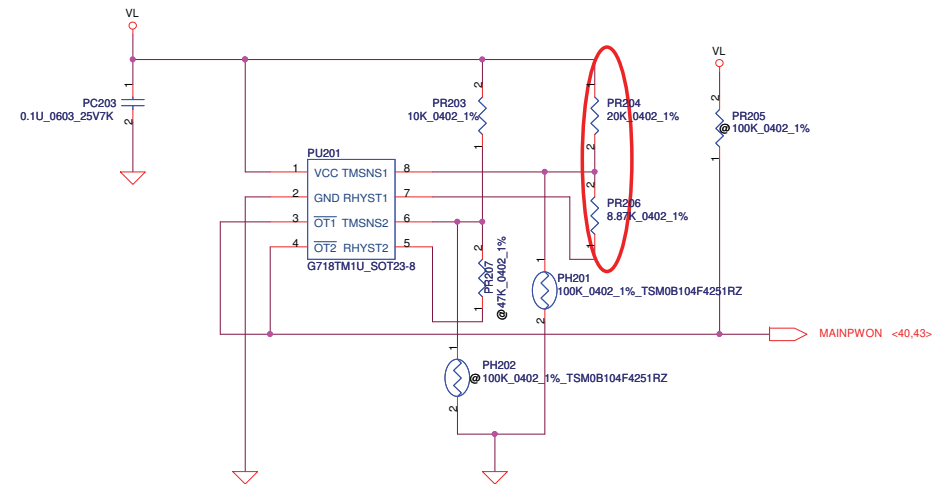
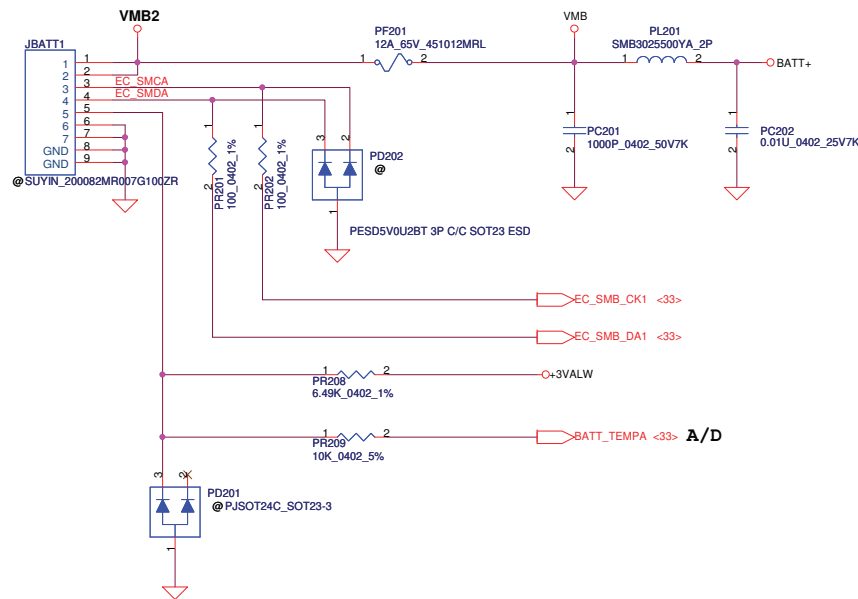
	Precharge detector		
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



RTC Battery

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				Date:	Tuesday, March 09, 2010	Sheet 40 of 48

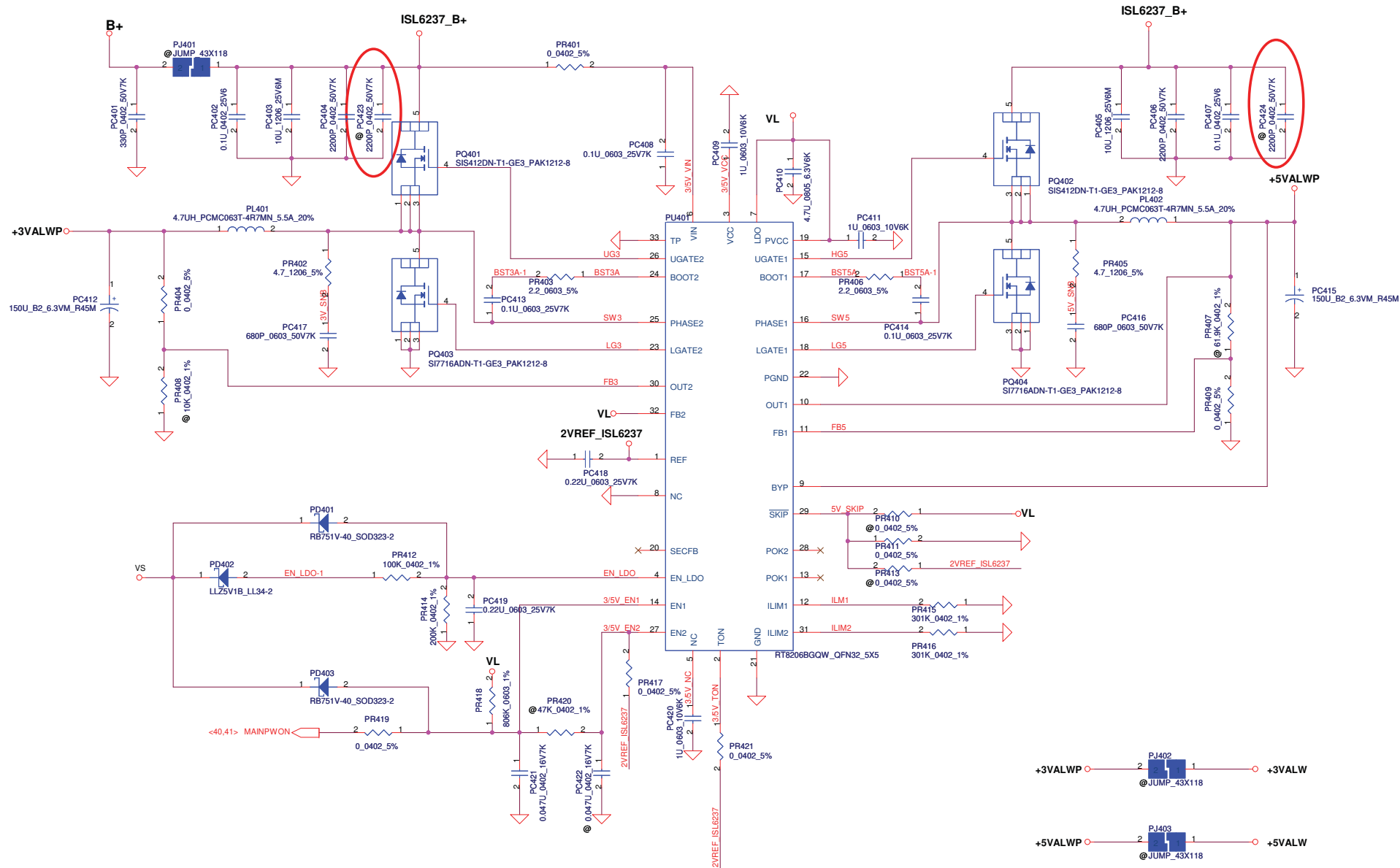
PH1 under CPU botten side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C



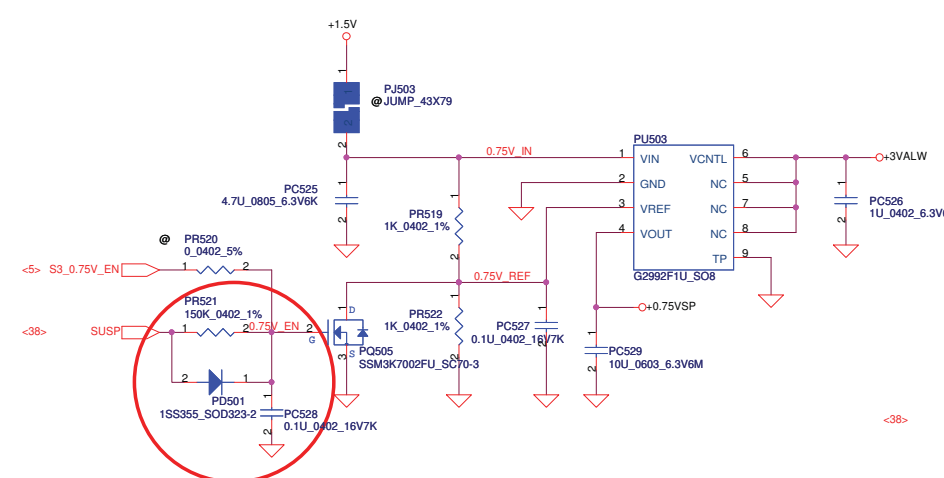
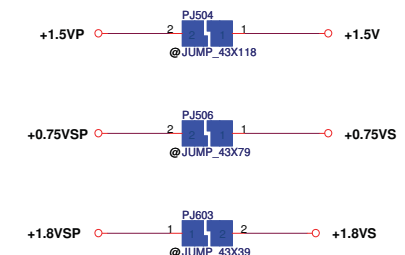
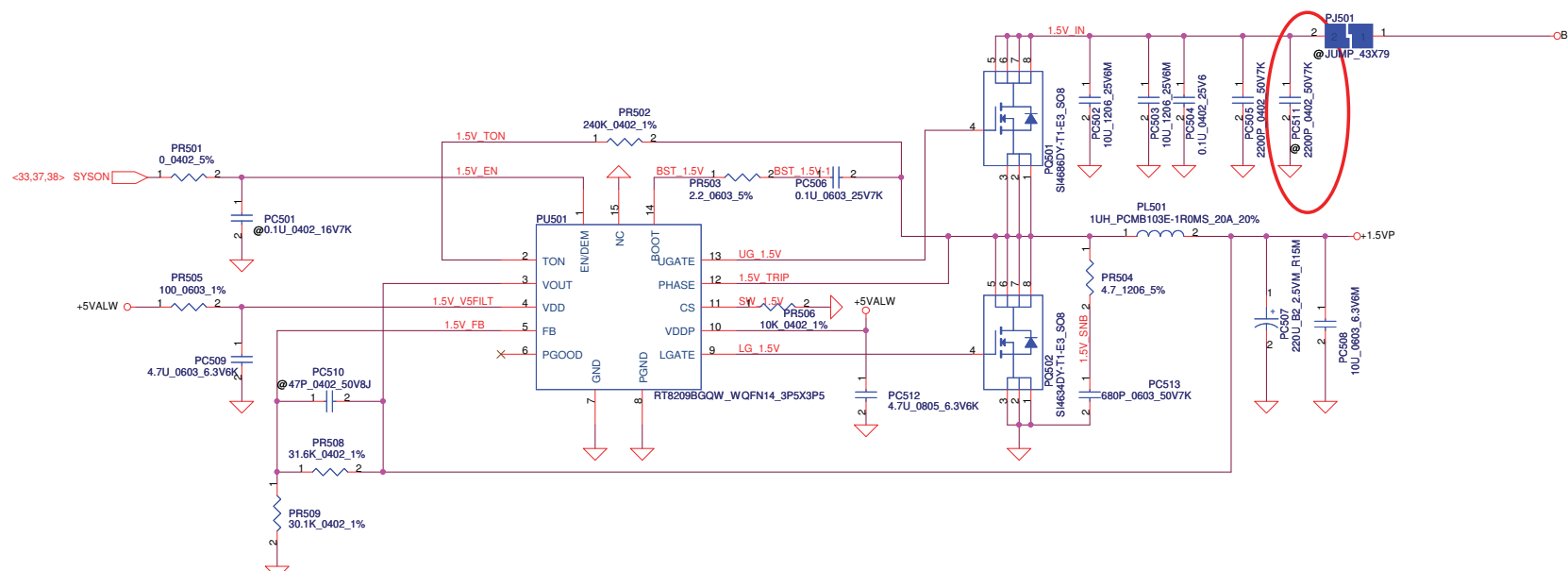
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Size		Document Number				Rev
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						0.1



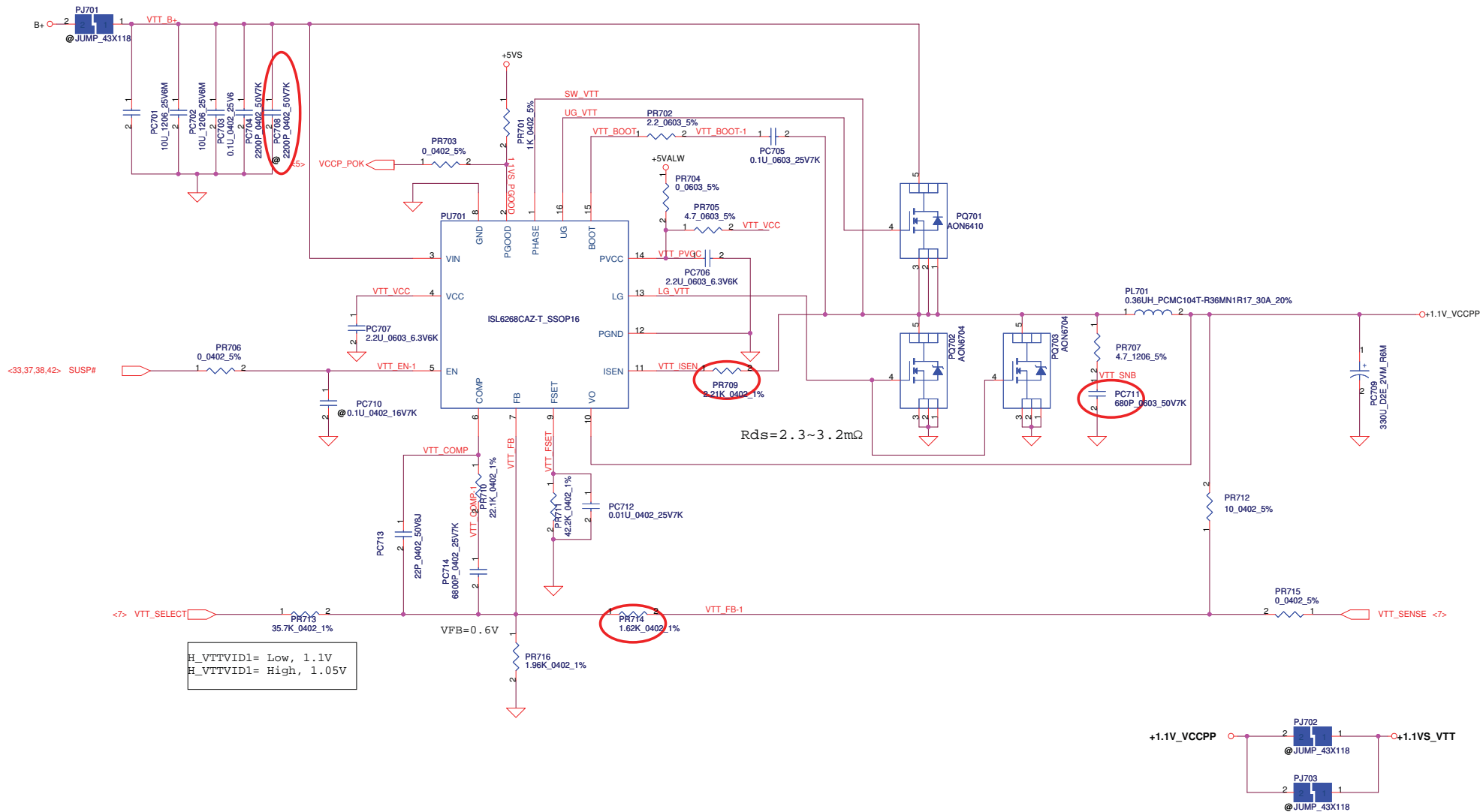
Date: Tuesday, March 09, 2010 Sheet 42 of 48



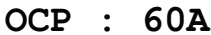
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009/10/10	Deciphered Date	2010/01/06	Title 3VALW/5VALW	
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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	For ESD	P41	Add PD202	2009.11.5	EVT
2	For HW request remove +1.05V's JUMP	P41	Remove +1.05V's JUMP	2009.11.6	EVT
3	Because limited high is not enough.	P47	Change PC907 from 220uF to 68uF	2009.11.6	EVT
4	Add PR830,PR831 for GFX_CORE sence.	P46	Add PR830,PR831 for GFX_CORE sence.	2009.11.17	EVT
5	Change Battery connent footprint.	P41	Change Battery connent footprint.	2009.11.17	EVT
6	Change PR521 from 0ohm to 150Kohm. Add PC528 on BOM.	P44	HW request	2009.11.25	EVT
7	Add PD501.	P44	HW request	2009.12.16	DVT
8	Reserve Cap. on B+ for RF.		RF request	2010.1.15	PVT
9	Change PR204 from 21.5Kohm to 20Kohm. Change PR206 from 9.76Kohm to 8.87Kohm.	P41	Thermal team request to change OTP temp. change from 92 degree to 95 degree.	2010.1.22	PVT
10					
11					
12					
13					
14					
15					
16					
17				20081022	

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